ZYNQ7000 FPGA Development Board AX7010

User Manual

ALINX

Version Record

Revision	Date	Release By	Description
Rev 1.0	2020-09-06	Rachel Zhou	First Release

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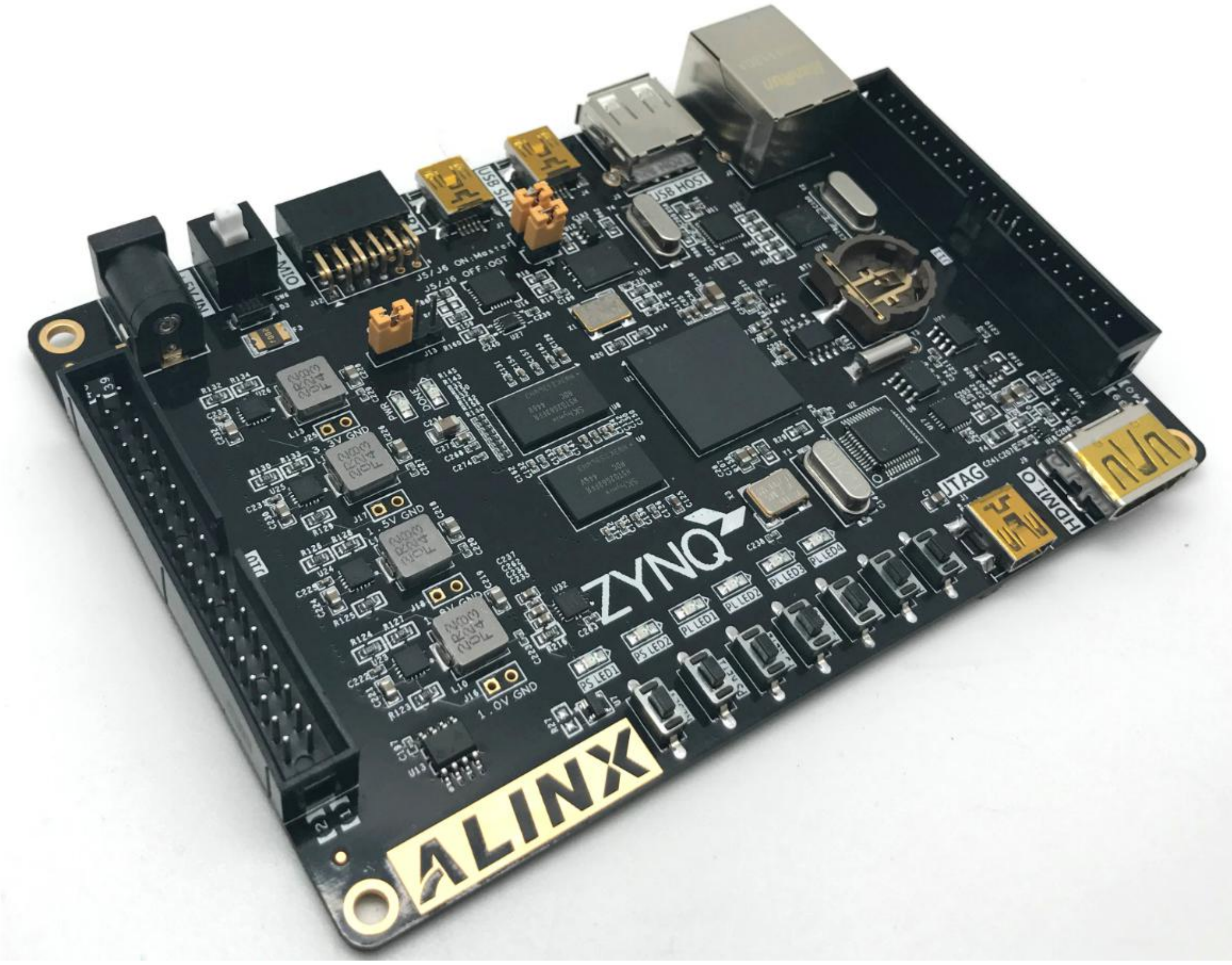
The ZYNQ7000 FPGA development platform uses XILINX's Zynq7000 SOC chip XC7Z010 solution, which uses ARM+FPGA SOC technology to integrate dual-core ARM Cortex-A9 and FPGA programmable logic on a single chip. The Xilinx Zynq7000 series XC7Z010-1CLG400C is used as the core processor, which has rich hardware resources and peripheral interfaces on ARM and FPGA respectively. Adhering to the "exquisite, practical, and concise" design concept, it is not only suitable for software verification of software workers, but also for hardware design of hardware developers, that is, system cooperation of software and hardware, and accelerate the development process of the project.



Part 1: FPGA Development Board Introduction

The AX7010 FPGA development board uses Xilinx's Zynq7000 series of chips, model XC7Z010-1CLG400C, in a 400-pin FBGA package. The ZYNQ7000 chip can be divided into a processor system part (PS) and a programmable logic part (PL). On the AX7010 development board, the PS and PL sections of the ZYNQ7000 are equipped with a wealth of external interfaces and devices for user convenience and functional verification. In addition, the Xilinx USB Cable downloader circuit is integrated on the AX7010 FPGA development board, so users can download and debug the AX7010 FPGA development board with a USB cable.

Figure 1-1 is the Schematic diagram of the entire AX7010 FPGA development board:

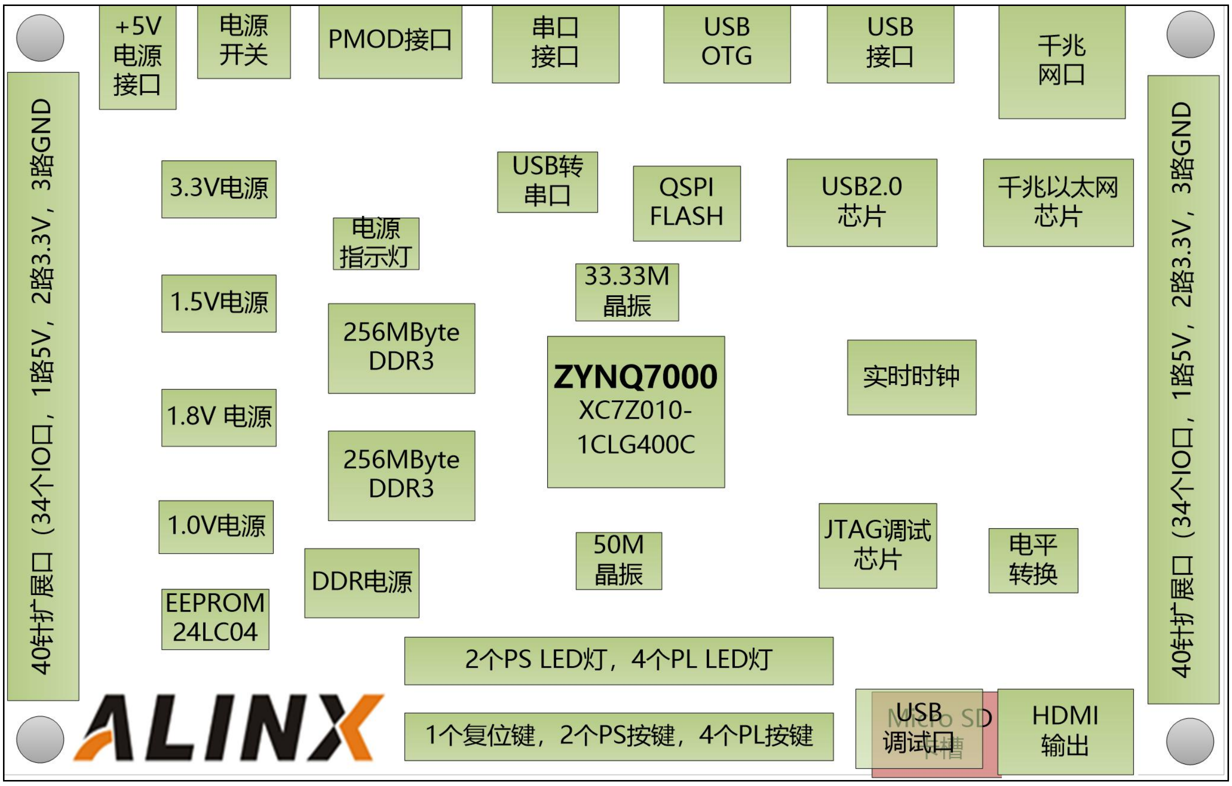


Figure 1-1: The Schematic Diagram of the AX7010

Through this diagram, you can see the interfaces and functions that the AX7010 FPGA Development Board contains:

- +5V power input, maximum 2A current protection
- Xilinx ARM+FPGA chip Zynq-7000 XC7Z010-1CLG400C
- DDR3

  Two large-capacity 2Gbit (A total of 4Gbit) high-speed DDR3 SDRAMs can be used as a cache for ZYNQ chip data or as a memory for the operating system
- QSPI FLASH

  A 256Mbit QSPI FLASH memory chip can be used as a Uboot file for ZYNQ chips, storage of system files and user data;
- Gigabit Ethernet Interface

  1-channel 10/100M/1000M Ethernet RJ45 interface for Ethernet data exchange with computers or other network devices.
- HDMI Input/Output Interface

  The 1-channel HDMI image video input and output interface, can realize 1080P video image transmission
- USB2.0 HOST Interface

  1-channel USB HOST interface, to connect with external USB slave devices, such as connecting a mouse, keyboard, USB flash drive etc. The USB interface uses a flat USB interface (USB Type A).
- USB OTG Interface

  1-channel high-speed USB2.0 OTG interface for OTG communication with PC or USB devices
- USB Uart Interface

  1-channel USB Uart interface for serial communication with PC or external devices
- RTC real time clock

  One of RTC real time clock with battery holders, battery model CR1220.
- EEPROM 24LC04

  One piece of IIC interface EEPROM 24LC04

- LED Light

  9 LEDs, 1 power indicator; 1 DONE configuration indicator; 2 serial communication indicators, 1 PS control LED, 4 PL control indicators.

- Button

  6 buttons, 2 buttons controlled by PS, 4 buttons controlled by PL.

- Clock

  An on-board 33.333Mhz active crystal oscillator provides a stable clock source for the PS system, a 50MHz active crystal oscillator that provides additional clocking for the PL logic

- 2-way 40-pin expansion port

  2-way 40-pin 0.1inch spacing expansion port for extending the IOs of ZYNQ PL parts, and can be connect to various ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.)

- 1-way 12-pin expansion port

  1-way 12-pin 0.1inch spacing expansion port for extending the MIO of ZYNQ PS system

- USB JTAG Interface

  One way USB JTAG port, debug and download ZYNQ system through USB cable and onboard JTAG circuit

- Micro SD card holder

  1-channel Micro SD card holder, to insert SD card for stores operating system images and file systems.

Part 2: Dimensional structure

The size of the development board is 130mm x 90mm, and the PCB is designed with an 8-layer board. There are 4 screw positioning holes around the board for fixing the development board. The holes diameter of the positioning hole is 3.5mm, and the dxf structure diagram is provided in the documents.

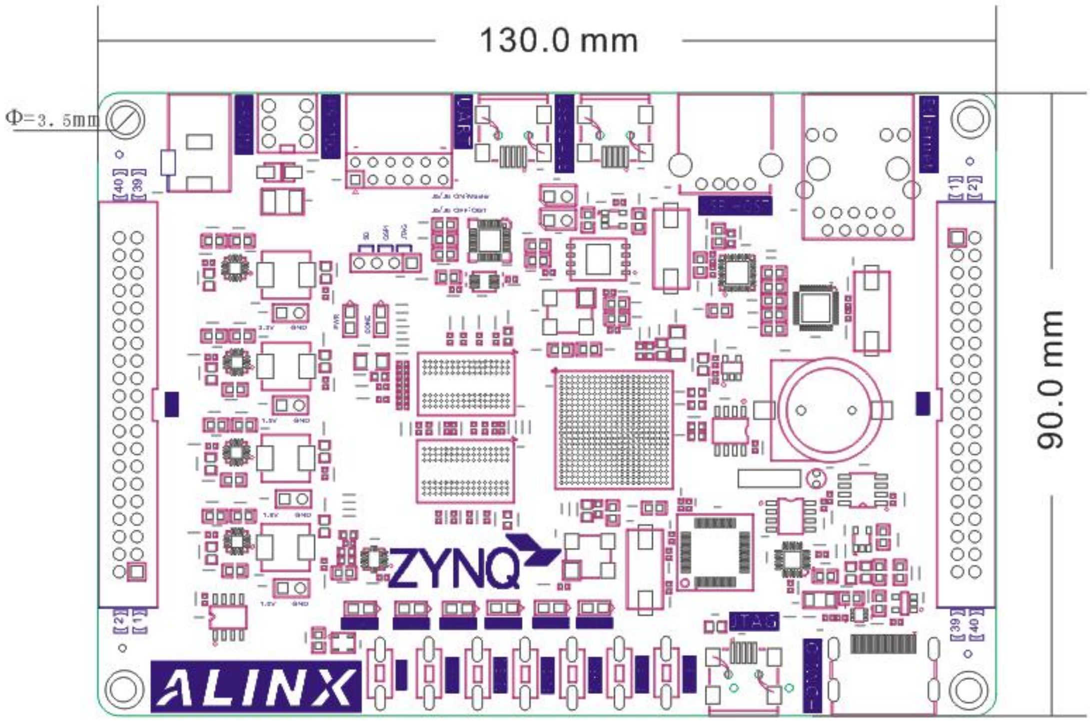


Figure 2-1: FPGA Size Dimension

Part 3: Power Supply

The power input voltage of the development board is DC5V, The schematic diagram of the power supply design on the AX7010 FPGA development board is shown in Figure 3-1

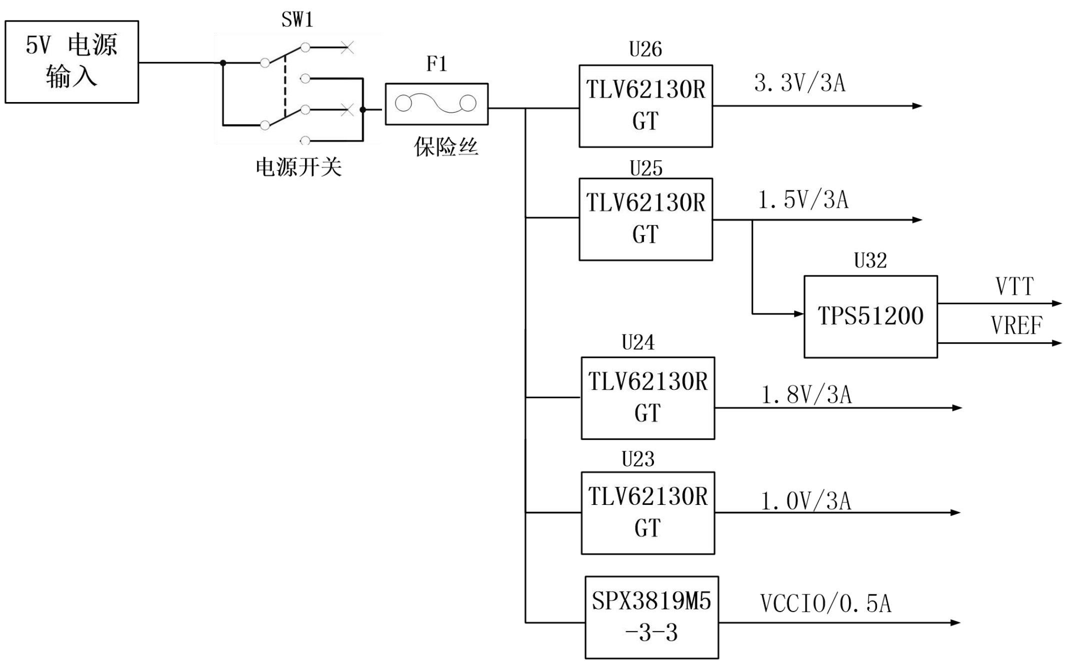


Figure 3-1: Power Supply Schematic

The development board is powered by +5V, and is converted into +3.3V, +1.5V, +1.8V, +1.0V four-way power supply through four DC/DC power supply chip TLV62130RGT. Each output current can be up to 3A. VCCIO power is generated by one LDO SPX3819M5-3-3, and VCCIO is mainly used to power the BANK35 of ZYNQ. By replacing other LDO chips, the BANK35's IO can be adapted to different voltage standards. VTT and VREF Voltage required by DDR3 are generated by 1.5V via TI's TPS51200. The functions of each power distribution are shown in the following table below:

Power Supply	Function
+1.0V	ZYNQ Core Voltage
+1.5V	DDR3, ZYNQ Bank502
+1.8V	ZYNQ auxiliary voltage, ZYNQ PLL, ZYNQ BANK501, VCCIO, Ethernet, USB 2.0
+3.3V	ZYNQ VCCIO, Gigabit Ethernet, Serial Port, HDMI, RTC, FLASH,EEPROM SD Card
VREF, VTT	DDR3
VCCIO	ZYNQ Bank35

Because the power supply of the ZYNQ FPGA has the power-on sequence requirements, in the circuit design, we have designed according to the power requirements of the chip. The power-on sequence is +1.0V->+1.8V->+1.5 V->+3.3V->VCCIO, circuit design to ensure the normal operation of the chip. Figure 3-2 shows the circuit design of the power supply:

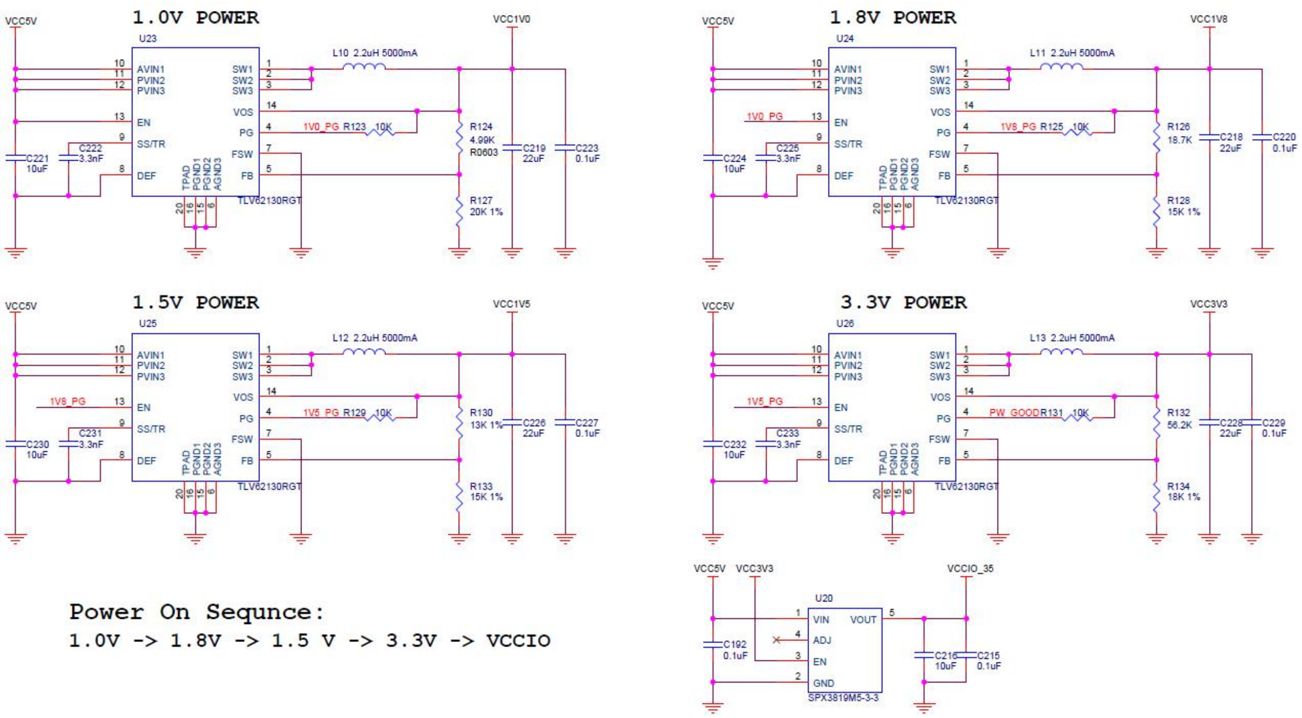


Figure 3-2: Power Supply Circuit

In the PCB design, an 8-layer PCB is used, and a separate power supply layer and GND layer are reserved, so that the power supply of the entire development board has very good stability. Test points for each power supply are reserved on the PCB so that the user can confirm the voltage on the board.

Figure 3-3: Test Points for Power supply on the Board

Part 4: ZYNQ Chip

The AX7010 FPGA development board uses Xilinx's Zynq7000 series chip, model XC7Z010-1CLG400C. The chip's PS system integrates two ARM CortexTM-A9 processors, AMBA® interconnects, internal memory, external memory interfaces and peripherals. These peripherals mainly include USB bus interface, Ethernet interface, SD/SDIO interface, I2C bus interface, CAN bus interface, UART interface, GPIO etc. The PS can operate independently and start up at power up or reset. Figure 2-1 detailed the Overall Block Diagram of the ZYNQ7000 Chip.

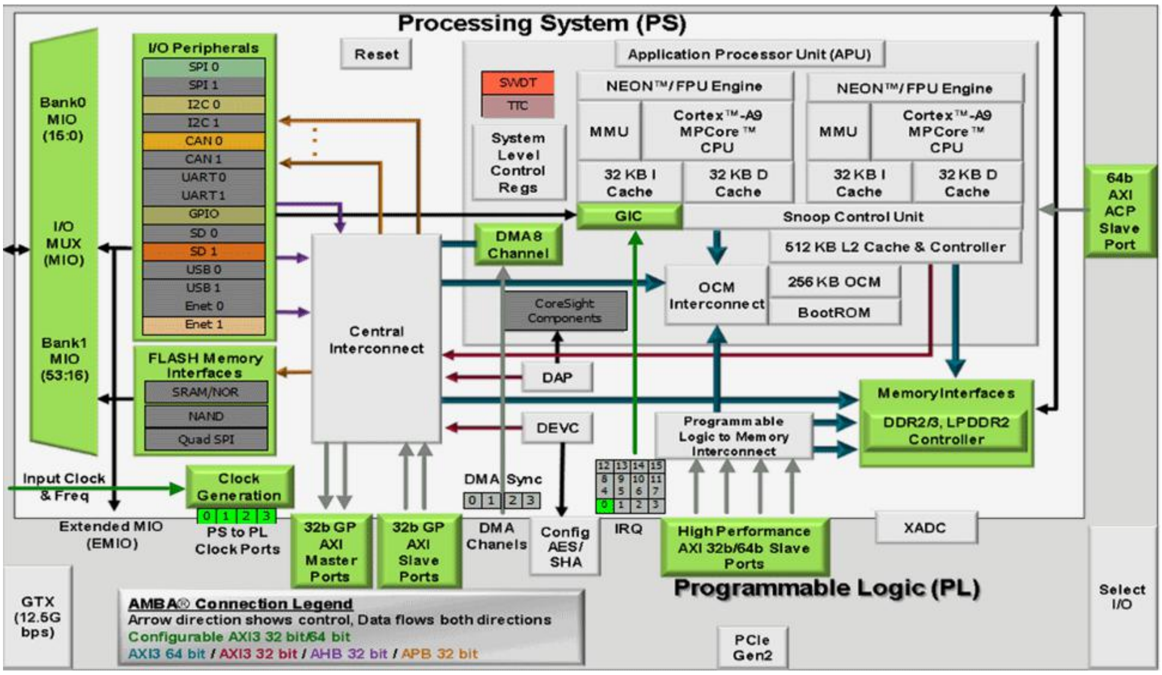


Figure 4-1: Overall Block Diagram of the ZYNQ7000 Chip

The main parameters of the PS system part are as follows:

- ARM dual-core CortexA9-based application processor, ARM-v7 architecture, up to 800MHz
- 32KB level 1 instruction and data cache per CPU, 512KB level 2 cache 2 CPU shares
- On-chip boot ROM and 256KB on-chip RAM
- External storage interface, support 16/32 bit DDR2, DDR3 interface
- Two Gigabit NIC support: divergent-aggregate DMA, GMII, RGMII, SGMII interface
- Two USB2.0 OTG interfaces, each supporting up to 12 nodes
- Two CAN2.0B bus interfaces
- Two SD card, SDIO, MMC compatible controllers

➢ 2 SPIs, 2 UARTs, 2 I2C interfaces

➢ 4 sets of 32bit GPIO, 54 (32+22) as PS system IO, 64 connected to PL

➢ High bandwidth connection within PS and PS to PL

The main parameters of the PL logic part are as follows:

- Logic Cells: 28K
- Look-up-tables (LUTs): 17600
- Flip-flops: 35200
- 18x25MACCs：80
- Block RAM：240KB
- Two AD converters for on-chip voltage, temperature sensing and up to 17 external differential input channels, 1MBPS

XC7Z010-1CLG400C chip speed grade is -1, commercial grade, package is BGA, pin pitch is 0.8mm the specific chip model definition of ZYNQ7000 series is shown in Figure 4-2

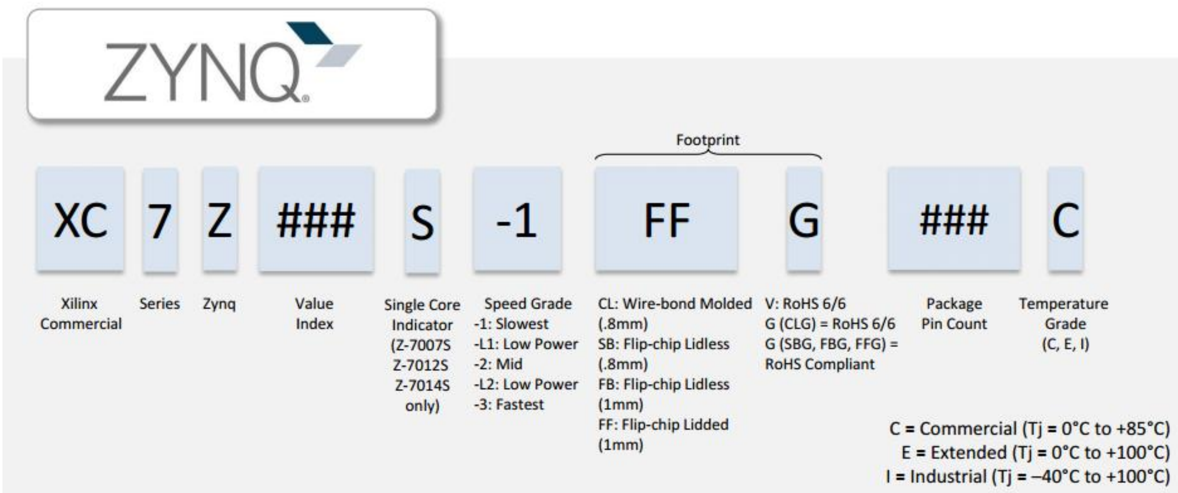


Figure 4-2: The Specific Chip Model Definition of ZYNQ7000 Series

The chip of the BGA package, the pin name is in the form of letters +

numbers, such as E3, G3 and so on. In the schematic, you see that the pin name is alpha + digit, which means it is a BGA package pin. Figure 4-3 detailed the XC7Z010 chip on the Board.

Figure 4-3: The XC7Z010 chip on the Board

Part 4.1: JTAG Interface

AX7010 FPGA development board, integrated JTAG download debugging circuit, users do not need to purchase additional Xilinx downloader. Only a USB cable can be used for ZYNQ development and debugging. On the AX7010 development board, a FTDI USB bridge chip FT232HL is used to realize USB and ZYNQ JTAG debug signals TCK, TDO, TMS, TDI for data communication. Figure 4-4 is the JTAG port schematic diagram.

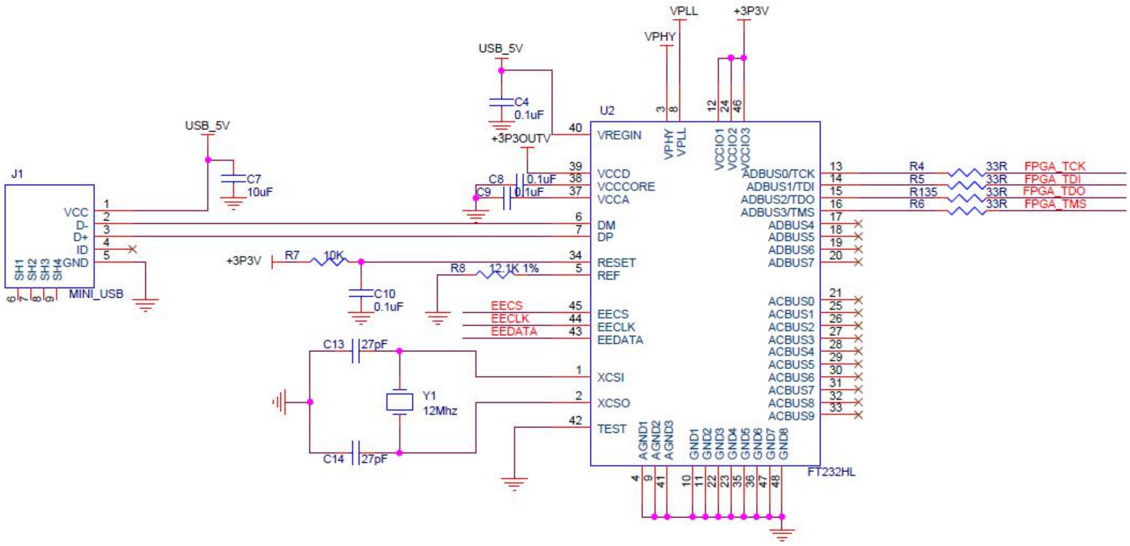


Figure 4-4: The JTAG port schematic

On the AX7010 FPGA development board, the JTAG interface is USB interface. Users can connect the PC and JTAG interface to the ZYNQ system debugging through the USB cable provided by us.

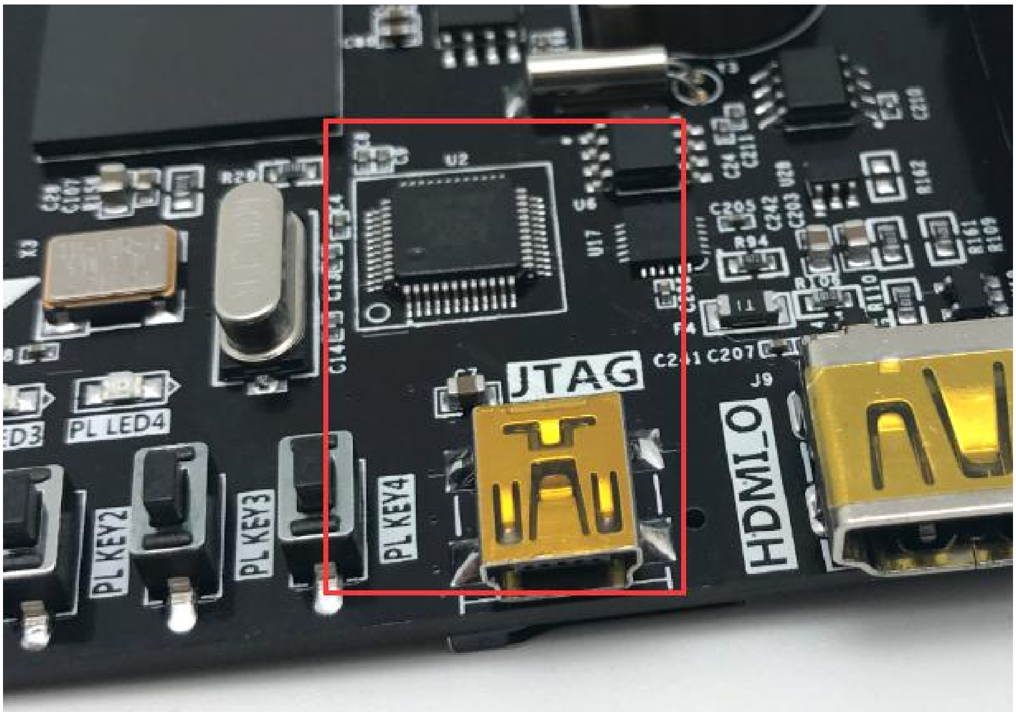


Figure 4-5: The JTAG port on the FPGA Board

Part 4.2: FPGA Power System

The power supply of the ZYNQ chip is divided into the PS system part and the PL logic part, and the two parts of the power supply work independently. The power supply of the PS system part and the power supply of the PL logic part have a power-on sequence. The abnormal power-on sequence may cause the ARM system and the FPGA system to not work properly.

The power supply for the PS section is VCCPINT, VCCPAUX, VCCPLL, and PS VCCO. VCCPINT is the PS core power supply pin, connected to 1.0V; VCCPAUX is the PS system auxiliary power supply pin, connected to 1.8V; VCCPLL is the PS internal clock PLL power supply pin, also connected to 1.8V; PS VCCO is BANK voltage, Including VCCO_MIO0, VCCO_MIO1 and VCCO_DDR, depending on the connected peripherals, the connected power supply will be different. On the AX7010 development board, VCC_MIO0 is connected to 3.3V, VCCO_MIO1 is connected to 1.8V, and VCCO_DDR is connected to 1.5V. The PS system requires that the power-up sequence be VCCPINT first, then VCCPAUX and VCCPLL, and finally PS VCCO. The order of power outages is reversed.

The power supply for the PL section is VCCINT, VCCBRAM, VCCAUX and VCCO. VCCPINT is the FPGA core power supply pin, connected to 1.0V; VCCBRAM is the power supply pin of the FPGA block RAM; connected to 1.0V; VCCAUX is the FPGA auxiliary power supply pin, connected to 1.8V; VCCO is the voltage of each BANK of PL, including BANK13, BANK34, BANK35, on the AX7010 development board, the voltage of BANK is connected to 3.3V. The PL system requires that the power-up sequence be VCCINT first, then VCCBRAM, then VCCAUX, and finally VCCO. If VCCINT and VCCBRAM have the same voltage, they can be powered up at the same time. The order of power outages is reversed.

Part 4.3: ZYNQ boot configuration

The AX7010 development platform supports three boot modes. The three boot modes are JTAG debug mode, QSPI FLASH and SD card boot mode. After the ZYNQ702 chip is powered up, it will detect the level of the responding MIO port to determine which startup mode. Users can select different startup modes through the J13 jumper on the FPGA development board. The J13 startup mode configuration is shown in Table 4-1.

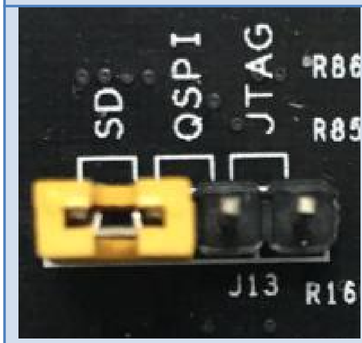
J13	Jump cap position	Start mode
	Connect the left two pins	SD Card
	Connect the middle two pins	QSPI FLASH
	Two pins connected to the right	JTAG

Table 4-1: startup mode configuration

Part 5: Clock Configuration

The AX7010 FPGA development board provides active clocks for the PS system and the PL logic, respectively. The PS system and PL logic can work independently.

Part 5.1: PS system clock source

The ZYNQ chip provides a 33.333MHz clock input to the PS section via the X1 crystal on the development board. The input of the clock is connected to the pin of the PS_CLK_500 of the BANK500 of the ZYNQ chip. The schematic diagram is shown in Figure 5-1:

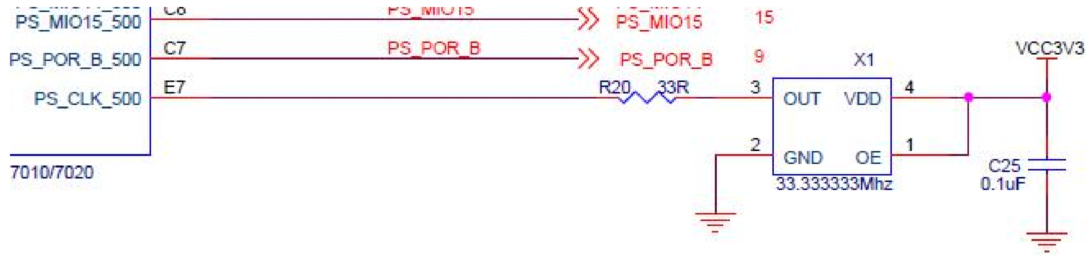


Figure 5-1: Active crystal oscillator to the PS section

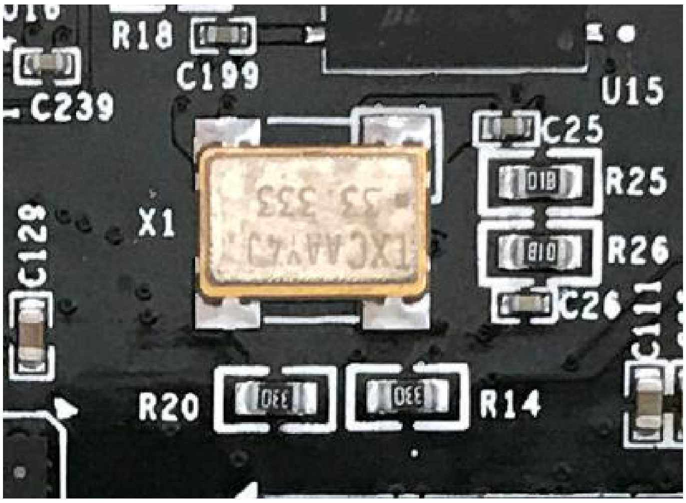


Figure 5-2: 33.333Mhz active Crystal Oscillator on the FPGA board

PS Clock Pin Assignment

Signal Name	ZYNQ Pin
PS_CLK	E7

Part 5.2: PL system clock source

The AX7010 FPGA development board provides a single-ended 50MHz PL system clock source with 3.3V supply. The crystal output is connected to the FPGA global clock (MRCC), which can be used to drive user logic circuit within the FPGA. The schematic diagram of the clock source is shown in Figure 5-3.

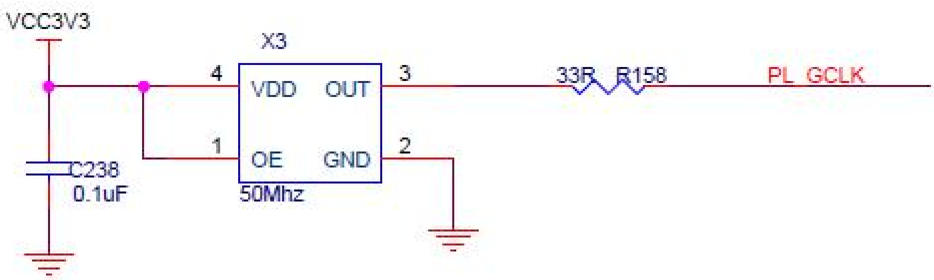


Figure 5-3: PL system clock source

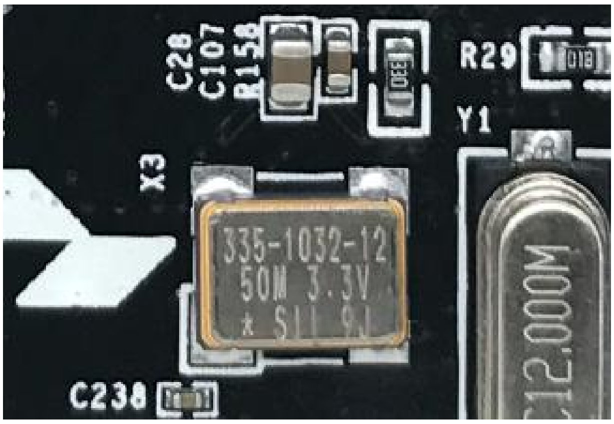


Figure 5-4: 50Mhz active crystal oscillator on the FPGA board

PL Clock pin assignment:

Signal Name	ZYNQ Pin
PL_GCLK	U18

Part 6：ZYNQ Processor System (PS) peripherals

ZYNQ is composed of the PS part of the ARM system and the PL part of the FPGA logic. Some peripherals on the development board are connected to the IO of the PS, and some peripherals are connected to the IO of the PL. First introduce the peripherals connected to the PS part.

Part 6.1: QSPI Flash

The AX7010 FPGA development board is equipped with a 256MBit

Quad-SPI FLASH chip, model W25Q256, which uses the 3.3V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 6-1.

Position	Model	Capacity	Factory
U6	W25Q256BV	32M Byte	Winbond

Table 6-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 6-1 shows the QSPI Flash in the schematic.

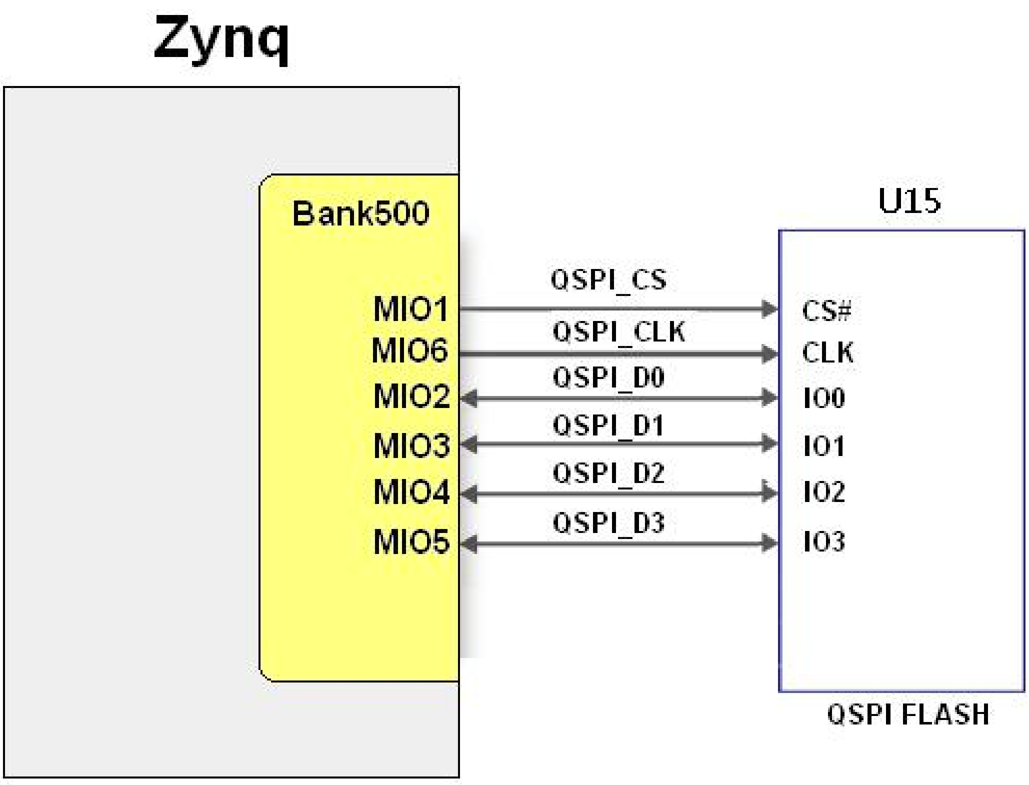


Figure 6-1: QSPI Flash Connection Diagram

Configure chip pin assignments:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
QSPI_SCK	PS_MIO6_500	A5
QSPI_CS	PS_MIO1_500	A7
QSPI_D0	PS_MIO2_500	B8
QSPI_D1	PS_MIO3_500	D6
QSPI_D2	PS_MIO4_500	B7
QSPI_D3	PS_MIO5_500	A6

Part 6.2: DDR3 DRAM

The AX7010 FPGA development board is equipped with two SKHynix 2Gbit DDR3 chips (total 4Gbit), model H5TQ2G63FFR (compatible with MT41J128M16HA-125). The DDR3 SDRAM has a maximum operating speed of 533MHz (data rate 1066Mbps), and two DDR3 memory systems are directly connected to the memory interface of the BANK 502 of the ZYNQ Processing System (PS). The specific configuration of DDR3 SDRAM is shown in Table 6-2.

Bit Number	Chip Model	Capacity	Factory
U8,U9	H5TQ2G63FFR-RDC	128M x 16bit	SKHynix

Table 6-2: DDR3 SDRAM Configuration

The hardware design of DDR3 requires strict consideration of signal integrity. We have fully considered the matching resistor/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR3.

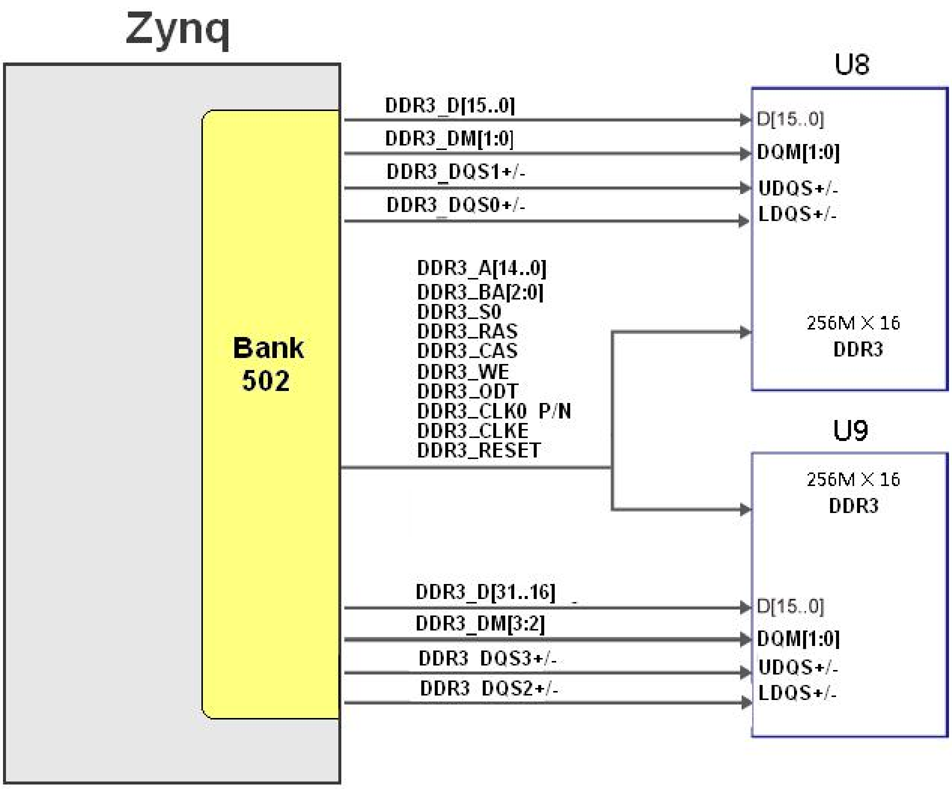


Figure 6-2: The Schematic Part of DDR3 DRAM

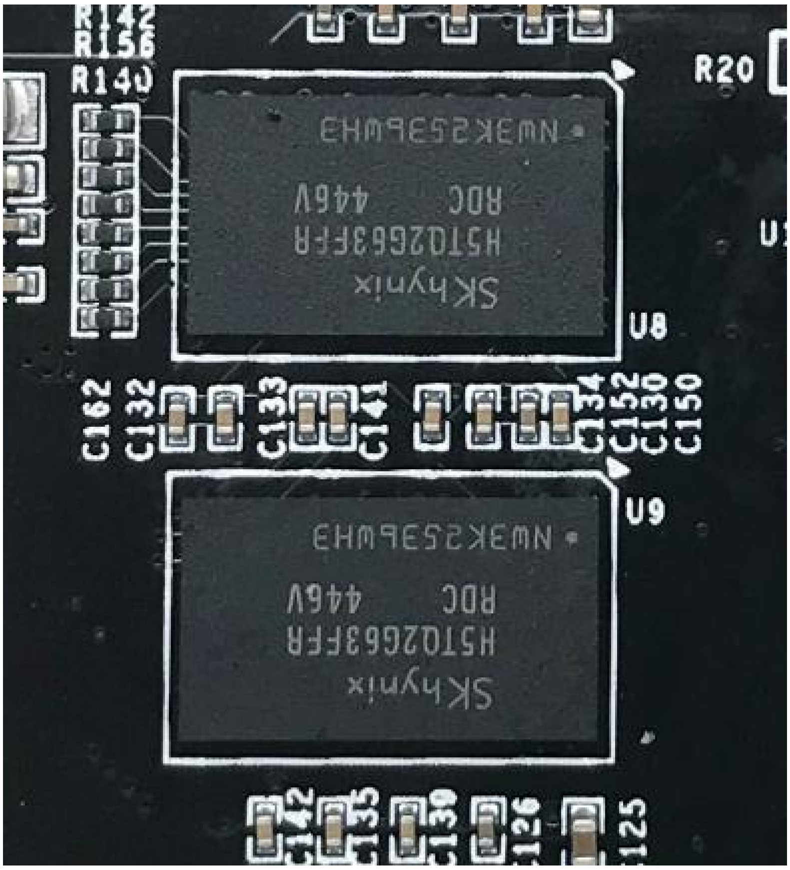


Figure 6-3: Two DDR3 DRAMs on the FPGA Board

DDR3 Pin Assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
DDR3_DQS0_P	PS_DDR_DQS_P0_502	C2
DDR3_DQS0_N	PS_DDR_DQS_N0_502	B2
DDR3_DQS1_P	PS_DDR_DQS_P1_502	G2
DDR3_DQS1_N	PS_DDR_DQS_N1_502	F2
DDR3_DQS2_P	PS_DDR_DQS_P2_502	R2
DDR3_DQS2_N	PS_DDR_DQS_N2_502	T2
DDR3_DQS3_P	PS_DDR_DQS_P3_502	W5
DDR3_DQS4_N	PS_DDR_DQS_N3_502	W4
DDR3_DQ[0]	PS_DDR_DQ0_502	C3
DDR3_DQ [1]	PS_DDR_DQ1_502	B3
DDR3_DQ [2]	PS_DDR_DQ2_502	A2
DDR3_DQ [3]	PS_DDR_DQ3_502	A4
DDR3_DQ [4]	PS_DDR_DQ4_502	D3
DDR3_DQ [5]	PS_DDR_DQ5_502	D1
DDR3_DQ [6]	PS_DDR_DQ6_502	C1
DDR3_DQ [7]	PS_DDR_DQ7_502	E1
DDR3_DQ [8]	PS_DDR_DQ8_502	E2
DDR3_DQ [9]	PS_DDR_DQ9_502	E3
DDR3_DQ [10]	PS_DDR_DQ10_502	G3
DDR3_DQ [11]	PS_DDR_DQ11_502	H3
DDR3_DQ [12]	PS_DDR_DQ12_502	J3
DDR3_DQ [13]	PS_DDR_DQ13_502	H2
DDR3_DQ [14]	PS_DDR_DQ14_502	H1
DDR3_DQ [15]	PS_DDR_DQ15_502	J1
DDR3_DQ [16]	PS_DDR_DQ16_502	P1
DDR3_DQ [17]	PS_DDR_DQ17_502	P3
DDR3_DQ [18]	PS_DDR_DQ18_502	R3
DDR3_DQ [19]	PS_DDR_DQ19_502	R1
DDR3_DQ [20]	PS_DDR_DQ20_502	T4
DDR3_DQ [21]	PS_DDR_DQ21_502	U4
DDR3_DQ [22]	PS_DDR_DQ22_502	U2
DDR3_DQ [23]	PS_DDR_DQ23_502	U3
DDR3_DQ [24]	PS_DDR_DQ24_502	V1
DDR3_DQ [25]	PS_DDR_DQ25_502	Y3

DDR3_DQ [26]	PS_DDR_DQ26_502	W1
DDR3_DQ [27]	PS_DDR_DQ27_502	Y4
DDR3_DQ [28]	PS_DDR_DQ28_502	Y2
DDR3_DQ [29]	PS_DDR_DQ29_502	W3
DDR3_DQ [30]	PS_DDR_DQ30_502	V2
DDR3_DQ [31]	PS_DDR_DQ31_502	V3
DDR3_DM0	PS_DDR_DM0_502	A1
DDR3_DM1	PS_DDR_DM1_502	F1
DDR3_DM2	PS_DDR_DM2_502	T1
DDR3_DM3	PS_DDR_DM3_502	Y1
DDR3_A[0]	PS_DDR_A0_502	N2
DDR3_A[1]	PS_DDR_A1_502	K2
DDR3_A[2]	PS_DDR_A2_502	M3
DDR3_A[3]	PS_DDR_A3_502	K3
DDR3_A[4]	PS_DDR_A4_502	M4
DDR3_A[5]	PS_DDR_A5_502	L1
DDR3_A[6]	PS_DDR_A6_502	L4
DDR3_A[7]	PS_DDR_A7_502	K4
DDR3_A[8]	PS_DDR_A8_502	K1
DDR3_A[9]	PS_DDR_A9_502	J4
DDR3_A[10]	PS_DDR_A10_502	F5
DDR3_A[11]	PS_DDR_A11_502	G4
DDR3_A[12]	PS_DDR_A12_502	E4
DDR3_A[13]	PS_DDR_A13_502	D4
DDR3_A[14]	PS_DDR_A14_502	F4
DDR3_BA[0]	PS_DDR_BA0_502	L5
DDR3_BA[1]	PS_DDR_BA1_502	R4
DDR3_BA[2]	PS_DDR_BA2_502	J5
DDR3_S0	PS_DDR_CS_B_502	N1
DDR3_RAS	PS_DDR_RAS_B_502	P4
DDR3_CAS	PS_DDR_CAS_B_502	P5
DDR3_WE	PS_DDR_WE_B_502	M5
DDR3_ODT	PS_DDR_ODT_502	N5
DDR3_RESET	PS_DDR_DRST_B_502	B4
DDR3_CLK_P	PS_DDR_CKP_502	L2
DDR3_CLK_N	PS_DDR_CKN_502	M2

DDR3_CKE	PS_DDR_CKE_502	N3

Part 6.3: Gigabit Ethernet Interface

The Ethernet chip uses Realtek's RTL8211E-VL Ethernet PHY chip to provide network communication services to users. The Ethernet PHY chip on the PS side is connected to the GPIO interface of the BANK501 of the PS side of ZYNQ. The RTL8211E-VL chip supports 10/100/1000 Mbps network transmission rate and communicates with the MAC layer of the Zynq7000 PS system through the RGMII interface. RTL8211E-VL supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and supports MDIO bus for PHY register management.

The RTL8211E-VL power-on will detect the level status of some specific IOs to determine their working mode. Table 6-3 describes the default setup information after the GPHY chip is powered up.

Configuration Pin	Instructions	Configuration value
PHYAD[2:0]	MDIO/MDC Mode PHY Address	PHY Address 为 001
SELRGV	RGMII 1.8V or 1.5V level selection	1.8V
AN[1:0]	Auto-negotiation configuration	10/100/1000 adaptive
RX Delay	RX clock 2ns delay	Delay
TX Delay	TX clock 2ns delay	Delay

Table 6-3: PHY chip default configuration value

When the network is connected to Gigabit Ethernet, the data transmission of ZYNQ and PHY chip RTL8211E-VL is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling samples of the clock.

When the network is connected to 100M Ethernet, the data transmission of ZYNQ and PHY chip RTL8211E-VL is communicated through RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

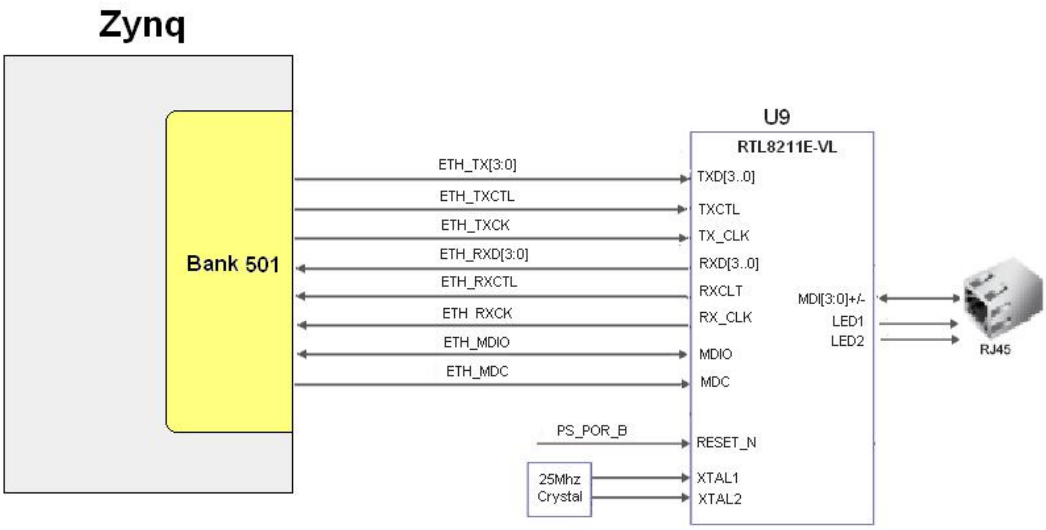


Figure 6-4: The connection of the ZYNQ and GPHY chip

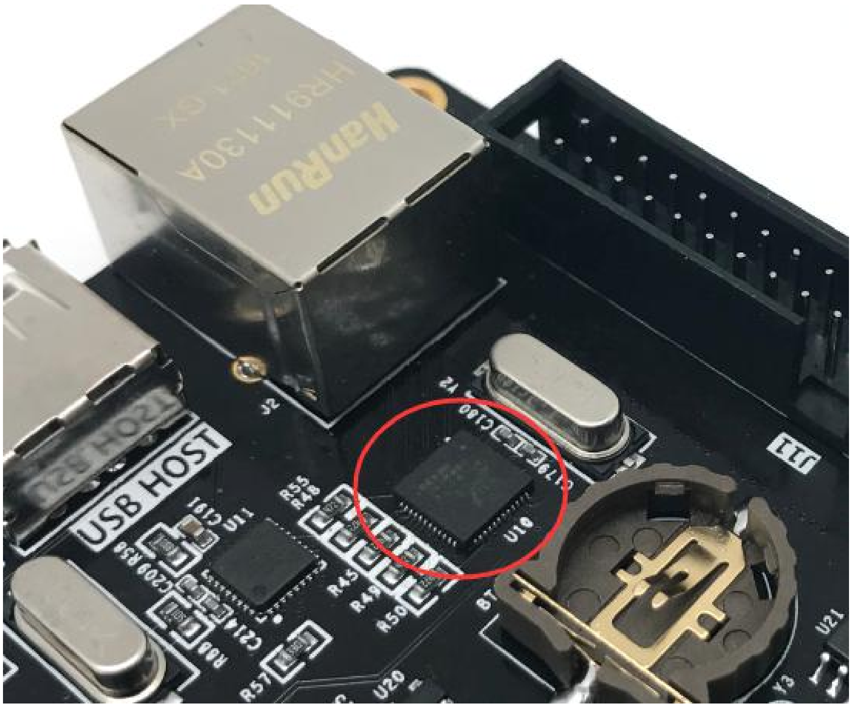


Figure 6-5: The GPHY chip on FPGA Board

The Gigabit Ethernet pin assignments are as follows：

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
ETH_GCLK	PS_MIO16_501	A19	RGMII Transmit Clock
ETH_TXD0	PS_MIO17_501	E14	Transmit data bit0
ETH_TXD1	PS_MIO18_501	B18	Transmit data bit1

ETH_TXD2	PS_MIO19_501	D10	Transmit data bit2
ETH_TXD3	PS_MIO20_501	A17	Transmit data bit3
ETH_TXCTL	PS_MIO21_501	F14	Transmit enable signal
ETH_RXCK	PS_MIO22_501	B17	RGMII Receive Clock
ETH_RXD0	PS_MIO23_501	D11	Receive data Bit0
ETH_RXD1	PS_MIO24_501	A16	Receive data Bit1
ETH_RXD2	PS_MIO25_501	F15	Receive data Bit2
ETH_RXD3	PS_MIO26_501	A15	Receive data Bit3
ETH_RXCTL	PS_MIO27_501	D13	Receive data valid signal
ETH_MDC	PS_MIO52_501	C10	MDIO Management clock
ETH_MDIO	PS_MIO53_501	C11	MDIO Management data

Part 6.4: USB2.0 Interface

There are 1 USB2.0 HOST interfaces on the AX7010 FPGA development board. The USB2.0 transceiver uses a 1.8V, high-speed USB3320C-EZK chip that supports the ULPI standard interface. ZYNQ's USB bus interface is connected to the USB3320C-EZK transceiver for high-speed USB2.0 Host mode and Slave mode data communication. The USB3320C's USB data and control signals are connected to the IO port of the BANK501 on the PS side of the ZYNQ chip. One 24MHz crystals provide clocks for the USB3320C.

The AX7010 FPGA development board provides users with two USB interfaces, one is the Host USB port and the other is the Slave USB port. They are a flat USB interface (USB Type A) and a micro USB interface (Micro USB), which are convenient for users to connect different USB peripherals. Users can switch between Host and Slave through J5 and J6 jumpers on the AX7010 FPGA development board. Table 6-4 shows the mode switching instructions:

J5,J6 Status	USB Mode	Instruction
J5 and J6 installation jumper caps	HOST Mode	FPGA Development board as the main device, USB port to connect the mouse, keyboard, USB and other slave peripherals

J5 and J6 not installation jumper caps	OTG/Slave Mode	FPGA Development board as a slave device, USB port to connect to the computer

Table 6-4: The mode Switching Instructions

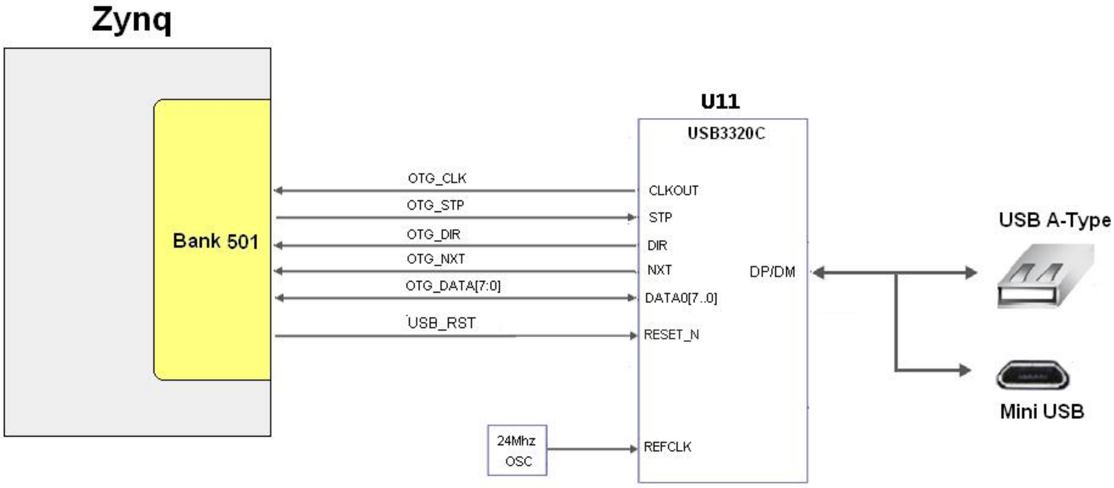


Figure 6-6: The connection between Zynq7000 and USB chip

Figure 6-7 shows the physical diagram of the USB2.0 part. U11 is USB3320C, J3 is the Host USB interface, and J4 is the Slave USB interface. Jumper caps J5 and J6 are used for Host and Slave mode selection.

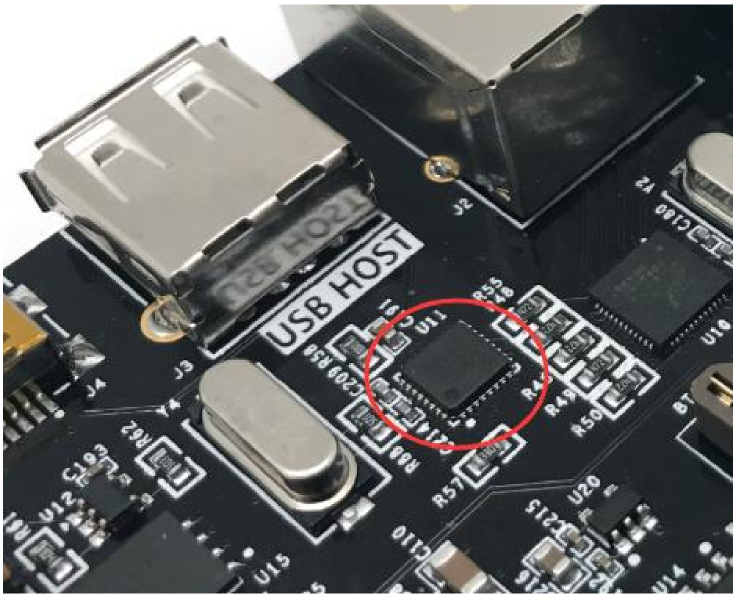


Figure 6-7: The USB3320C chip on the FPGA Board

USB2.0 Pin Assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
OTG_DATA4	PS_MIO28_501	C16	USB Data Bit4
OTG_DIR	PS_MIO29_501	C13	USB Data Direction Signal
OTG_STP	PS_MIO30_501	C15	USB Stop Signal
OTG_NXT	PS_MIO31_501	E16	USB Next Data Signal
OTG_DATA0	PS_MIO32_501	A14	USB Data Bit0
OTG_DATA1	PS_MIO33_501	D15	USB Data Bit1
OTG_DATA2	PS_MIO34_501	A12	USB Data Bit2
OTG_DATA3	PS_MIO35_501	F12	USB Data Bit3
OTG_CLK	PS_MIO36_501	A11	USB Clock Signal
OTG_DATA5	PS_MIO37_501	A10	USB Data Bit5
OTG_DATA6	PS_MIO38_501	E13	USB Data Bit6
OTG_DATA7	PS_MIO39_501	C18	USB Data Bit7
OTG_RESETN	PS_MIO46_501	D16	USB Reset Signal

Part 6.5: USB to Serial Port

The AX7010 FPGA development board uses the USB to UART chip of Silicon Labs CP2102GM. The USB interface uses the Micro USB interface. Users can connect to the PC for serial communication using a Micro USB cable.

The TX/RX signal of the UART is connected to the signal of the PS BANK501 of the ZYNQ EPP. Since the VCCMIO of the BANK is set to 1.8V, the data level of the CP2102GM is 3.3V, which is connected by the TXS0102DCUR level conversion chip. Figure 6-8 detailed the schematic diagram of the CP2102GM and ZYNQ connections

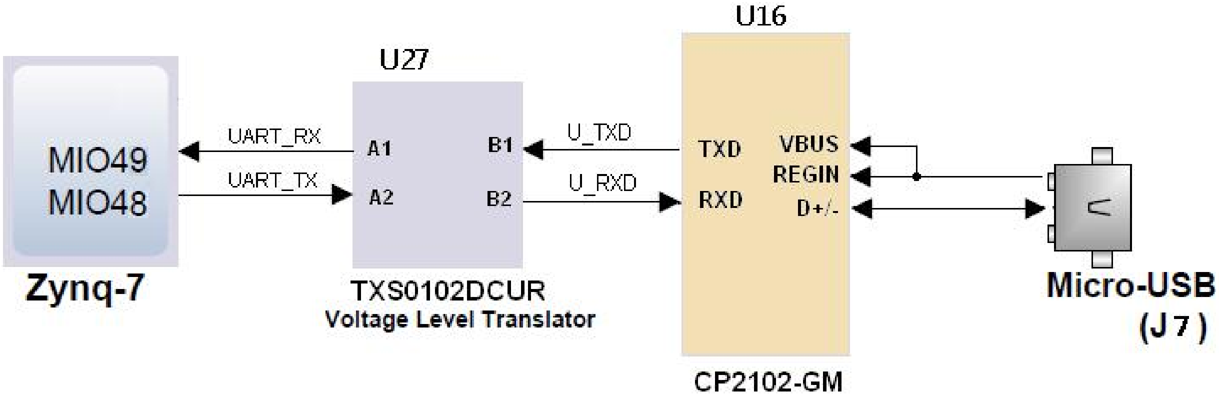


Figure 6-8: USB to serial port schematic

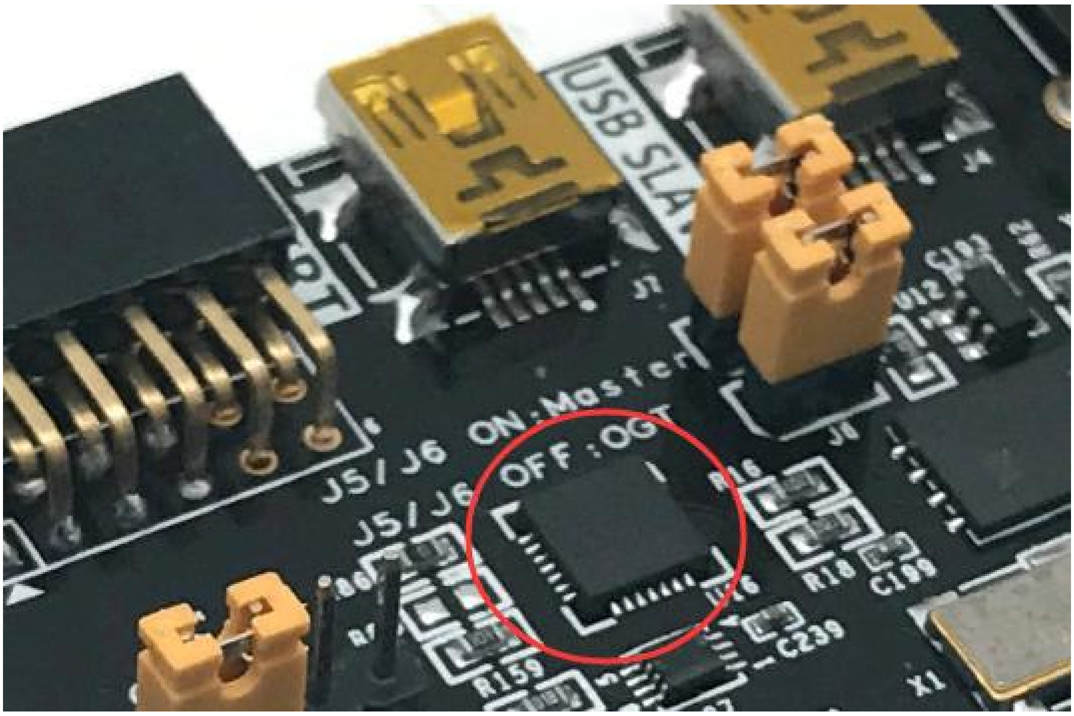


Figure 6-9: CP2102GM chip on the FPGA Board

USB to serial port ZYNQ pin assignment:

Signal name	ZYNQ Pin Name	ZYNQ Pin Number	Description
UART_TX	PS_MIO48_501	B12	Uart data input
UART_RX	PS_MIO49_501	C12	Uart data output

Silicon Labs provides virtual COM port (VCP) drivers for host PCs. These drivers allow the CP2102GM USB-UART bridge device to be displayed as a

COM port in communications application software, such as TeraTerm or HyperTerminal. The VCP device driver must be installed before the PC host establishes communication with the AX7010 FPGA development board.

Part 6.6: SD Card Slot

The AX7010 FPGA Development Board contains a Micro SD card interface to provide user access to the SD card memory, the BOOT program for the ZYNQ chip, the Linux operating system kernel, the file system and other user data files.

The SDIO signal is connected to the IO signal of the PS BANK501 of ZYNQ. Since the VCCMIO of the BANK is set to 1.8V, but the data level of the SD card is 3.3V, connected through the TXS02612 level shifter. The schematic of the Zynq7000 PS and SD card connector is shown in Figure 6-10:

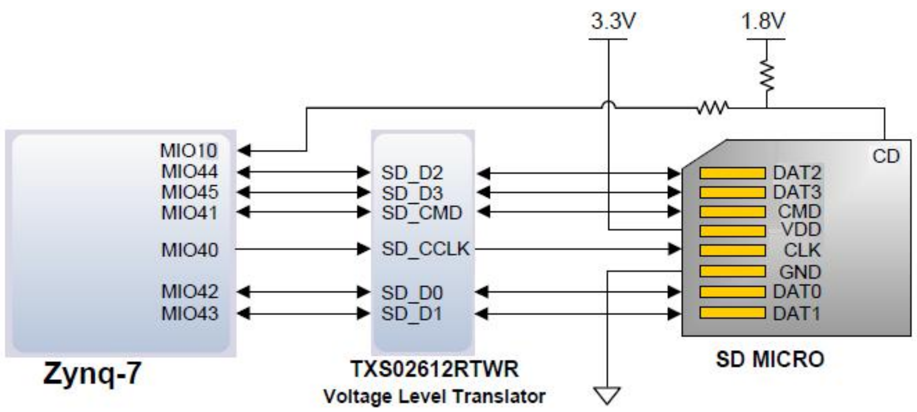


Figure 6-10: SD Card Connection Diagram

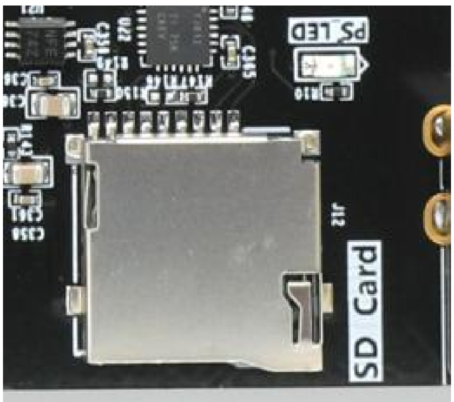


Figure 6-11: SD Card Slot on the FPGA Board

SD card slot pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
SD_CLK	PS_MIO40	D14	SD Clock Signal
SD_CMD	PS_MIO41	C17	SD Command Signal
SD_D0	PS_MIO42	E12	SD Data0
SD_D1	PS_MIO43	A9	SD Data1
SD_D2	PS_MIO44	F13	SD Data2
SD_D3	PS_MIO45	B15	SD Data3
SD_CD	PS_MIO47	B14	SD Card Insertion Signal

Part 6.7: PS PMOD connector

The AX7010 development board reserves a 12-pin 2.54mm pitch PMOD interface (J12) for connecting the IO of the BANK500 and external modules or circuits. Because the IO is 3.3V standard, the signal of the connected external devices and circuits also requires a 3.3V level standard. The schematic diagram of the PMOD connector is shown in Figure 6-12.

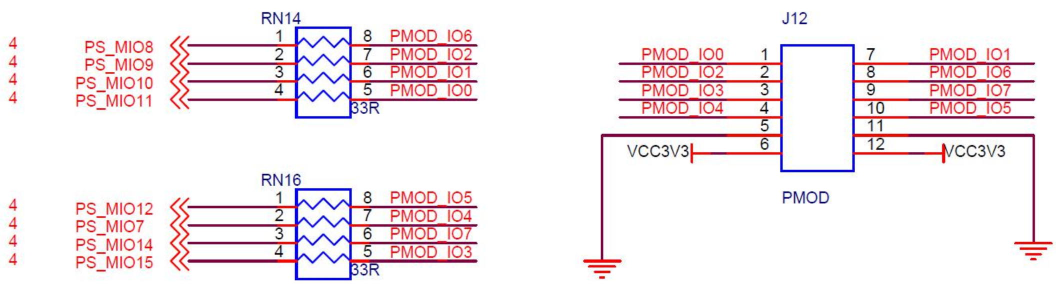


Figure 6-12: PS PMOD connector Schematic

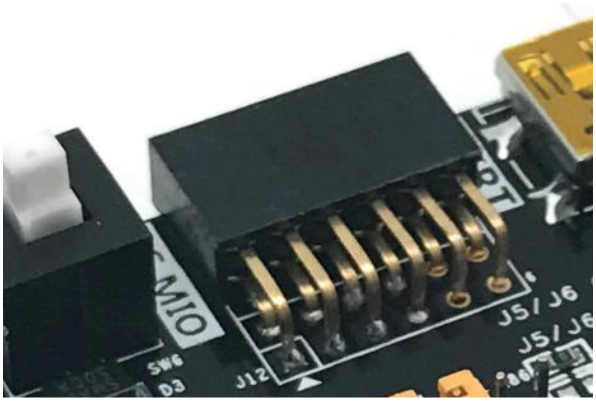


Figure 6-13: PS PMOD connector on the FPGA board

PS PMOD Connector pin assignment:

PMOD Pin	Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PIN1	PMOD_IO0	PS_MIO11_500	C6
PIN2	PMOD_IO2	PS_MIO9_500	B5
PIN3	PMOD_IO3	PS_MIO15_500	C8
PIN4	PMOD_IO4	PS_MIO7_500	D8
PIN5	GND	-	-
PIN6	+3.3V	-	-
PIN7	PMOD_IO1	PS_MIO10_500	E9
PIN8	PMOD_IO6	PS_MIO8_500	D5
PIN9	PMOD_IO7	PS_MIO14_500	C5
PIN10	PMOD_IO5	PS_MIO12_500	D9
PIN11	GND	-	-
PIN12	+3.3V	-	-

Part 6.8: User LEDs

On the AX7010 FPGA development board, two LEDs are connected to the BANK500 IO in the PS section, and the user can use these two LEDs to debug the program. When the BANK500 IO voltage is high, the LED light is off, and when the BANK500 IO voltage is low, the LED will be illuminated. A schematic diagram of the ZYNQ BANK500 IO and LEDs connections is shown in Figure 6-14:

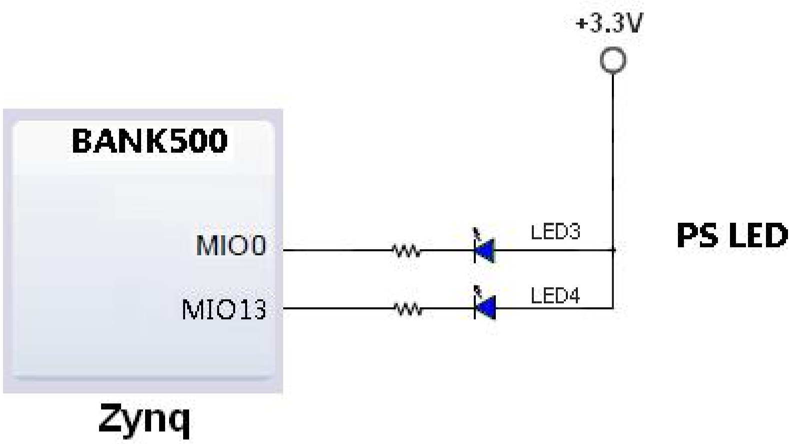


Figure 6-14: User LEDs Schematic

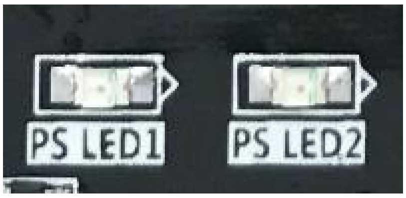


Figure 6-15: PS User LEDs on the FPGA Board

PS User LEDs pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
MIO0_LED	PS_MIO0_500	E6	PS User LED LED1
MIO13_LED	PS_MIO13_500	E8	PS User LED LED2

Part 6.9: User Buttons

On the AX7010 development board, two user buttons are connected to the BANK501 IO in the PS section. The user can use these two user buttons to test the input signal and interrupt trigger. In the circuit design, when the button is pressed, the signal voltage input to the ZYNQ BANK501 IO is low, and when it is not pressed, the signal is high. A schematic diagram of the ZYNQ BANK501 IO and button connections is shown in Figure 6-16:

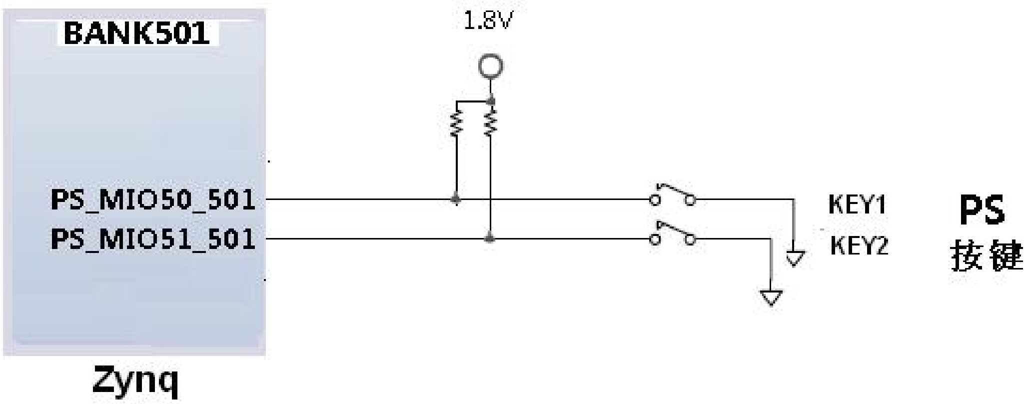


Figure 6-16: PS User Buttons Schematic

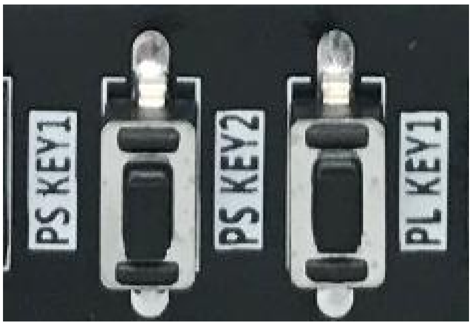


Figure 6-17: PS User Buttons on the FPGA Board

PS User LEDs pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
MIO_KEY1	PS_MIO50_501	B13	PS User Button KEY1
MIO_KEY2	PS_MIO51_501	B9	PS User Button KEY2

Part 7：ZYNQ Programmable Logic (PL) peripherals

Part 7.1: HDMI Interface

HDMI, full name is the high definition multimedia video output interface. AX7010 development board, differential IO of FPGA is directly connected to the differential signal and clock of HDMI interface, realizes differential transfer of HMDI signal in parallel and encodes and decodes in FPGA, realizes transmission solution of DMI digital video input and output, up to 1080P@ 60Hz input and output functions.

The HDMI signal is connected to the BANK34 of the PL part of ZYNQ. Figure 7-1 is the HDMI design schematic. When the development board is used as an HDMI display device (HDMI IN), the HDMI signal is used as an input, and the HPD (hot plug detect) signal is used as an output. When the development board is used as an HDMI master (HDMI OUT), the opposite is true.

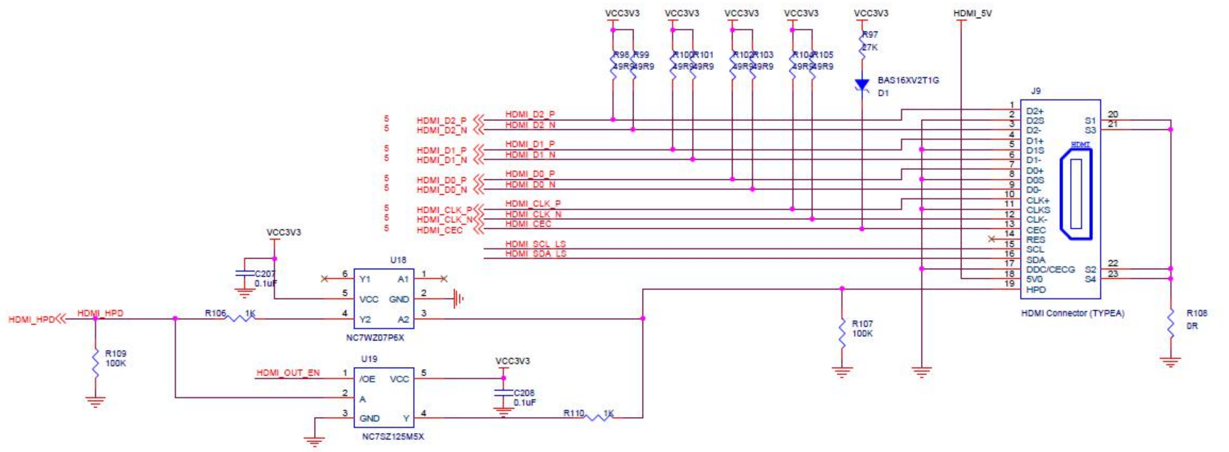


Figure 7-1: HDMI interface design schematic

When the development board is used as an HDMI main unit (HDMI OUT), it needs to supply a +5V power supply to the HDMI display device. The power output control circuit is shown in Figure 7-2.

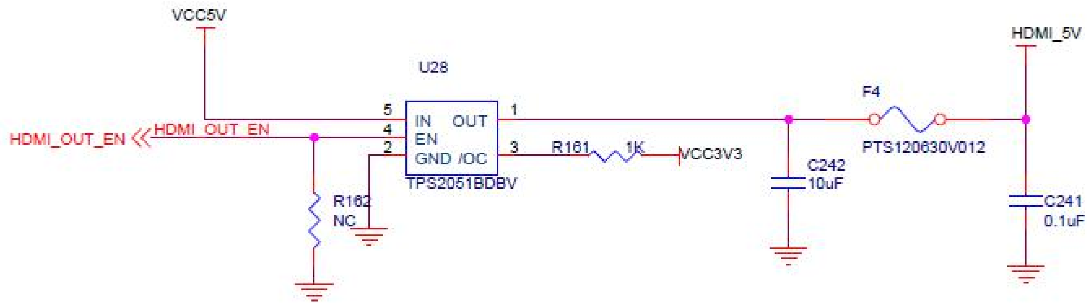


Figure 7-2: HDMI 5V output circuit

The HMDI master device reads the EDID device information of the HDMI display device through the IIC bus. The pin level of the FPGA is 3.3V, but the level of HDMI is +5V, which requires the level conversion chip GTL2002D to connect. The conversion circuit of IIC is shown in Figure 7-3.

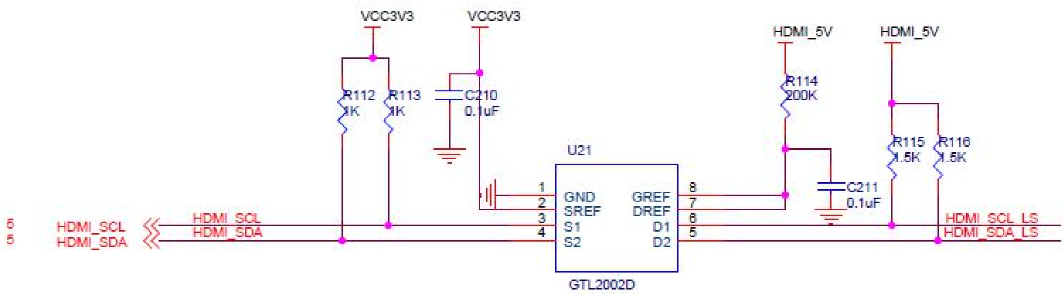


Figure 7-3: GTL2002D level conversion circuit

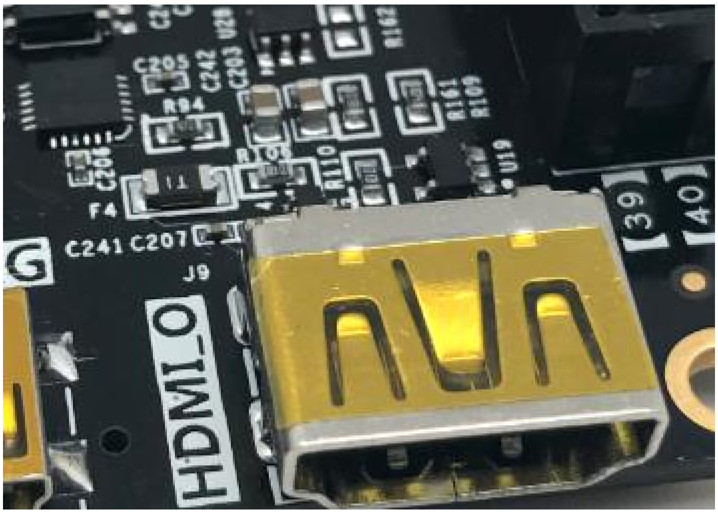


Figure 7-4: HDMI Interface on the FPGA Board

HDMI Interface Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
HDMI_CLK_P	IO_L13P_T2_MRCC_34	N18	HDMI Clock Signal positive
HDMI_CLK_N	IO_L13N_T2_MRCC_34	P19	HDMI Clock Signal negative
HDMI_D0_P	IO_L16P_T2_34	V20	HDMI data 0 positive
HDMI_D0_N	IO_L16N_T2_34	W20	HDMI data 0 negative
HDMI_D1_P	IO_L15P_T2_DQS_34	T20	HDMI data 1 positive
HDMI_D1_N	IO_L15N_T2_DQS_34	U20	HDMI data 1 negative
HDMI_D2_P	IO_L14P_T2_SRCC_34	N20	HDMI data 2 positive
HDMI_D2_N	IO_L14N_T2_SRCC_34	P20	HDMI data 2 negative
HDMI_SCL	IO_L20N_T3_34	R18	HDMI IIC Clock
HDMI_SDA	IO_L19P_T2_34	R16	HDMI IIC Data
HDMI_CEC	IO_L17P_T2_34	Y18	HDMI remote control signal
HDMI_HPD	IO_L17N_T2_34	Y19	HDMI hot plug detection signal
HDMI_OUT_EN	IO_L18P_T2_34	V16	HDMI power output control

Part 7.2: EEPROM 24LC04

AX7010 FPGA development board contains an EEPROM, model 24LC04, and has a capacity of 4Kbit (2*256*8bit). It consists of two 256-byte blocks and communicates via the IIC bus. The onboard EEPROM is to learn how to communicate with the IIC bus. The I2C signal of the EEPROM is connected to the BANK14 IO port on the ZYNQ PL side. Figure 7-5 below shows the design of the EEPROM

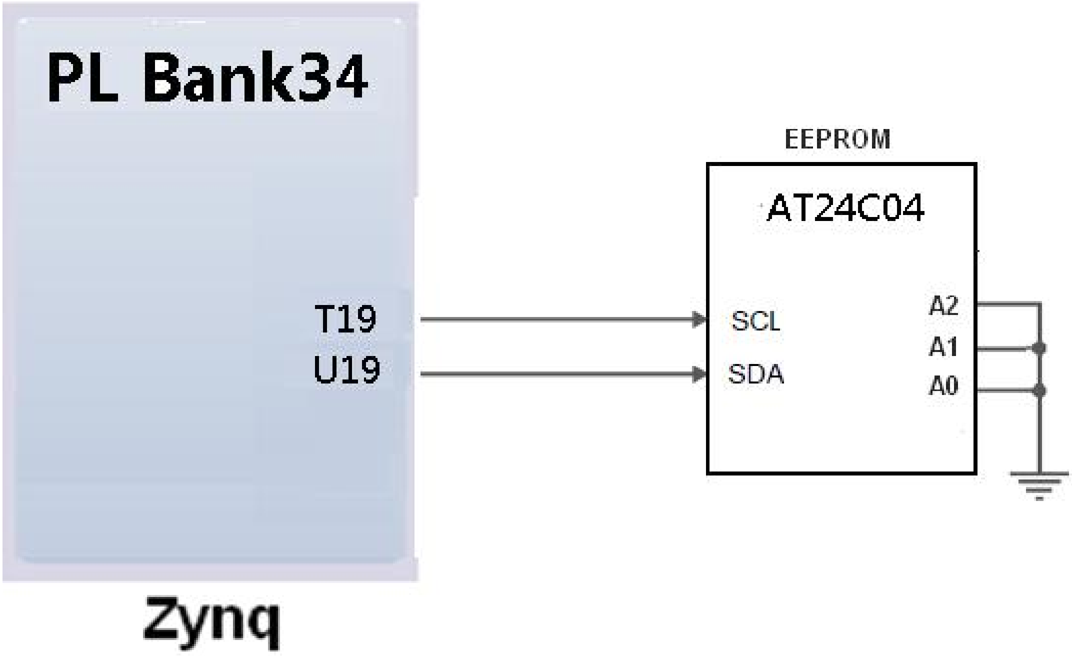


Figure 7-5: EEPROM Schematic

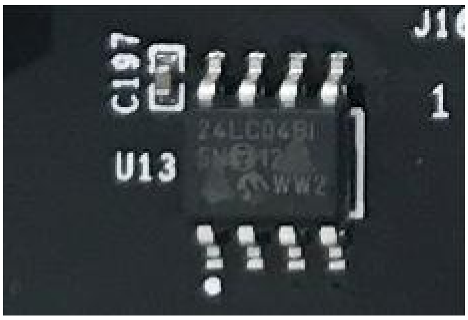


Figure 7-6: EEPROM on the FPGA Board

EEPROM Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
EEPROM_I2C_SCL	IO_25_34	T19	IIC Clock Signal
EEPROM_I2C_SDA	IO_L12N_T1_MRCC_34	U19	IIC Data Signal

Part 7.3: Real Time Clock DS1302

The development board contains a real-time clock RTC chip, model DS1302, which provides a calendar function up to 2099, with days, minutes, minutes, seconds and weeks. If time is needed in the system, then the RTC needs to be involved in the product. It needs to connect a 32.768KHz passive clock to provide an accurate clock source to the clock chip, so that the RTC can accurately provide clock information to the product. At the same time, in order to power off the product, the real-time clock can still operate normally. Generally, a battery is required to supply power to the clock chip. In Figure 7-8, the BT1 is the battery holder, and the button battery (**model CR1220, voltage is 3V**) is placed. After the system is turned off, the button battery can also supply power to the DS1302. This way, regardless of whether the product is powered or not, the DS1302 will operate normally without interruption and provide continuous time information. The RTC interface signal is connected to the IO ports of BANK34 and BANK35 on the ZYNQ PL side. Figure 7-7 shows the design of the DS1302:

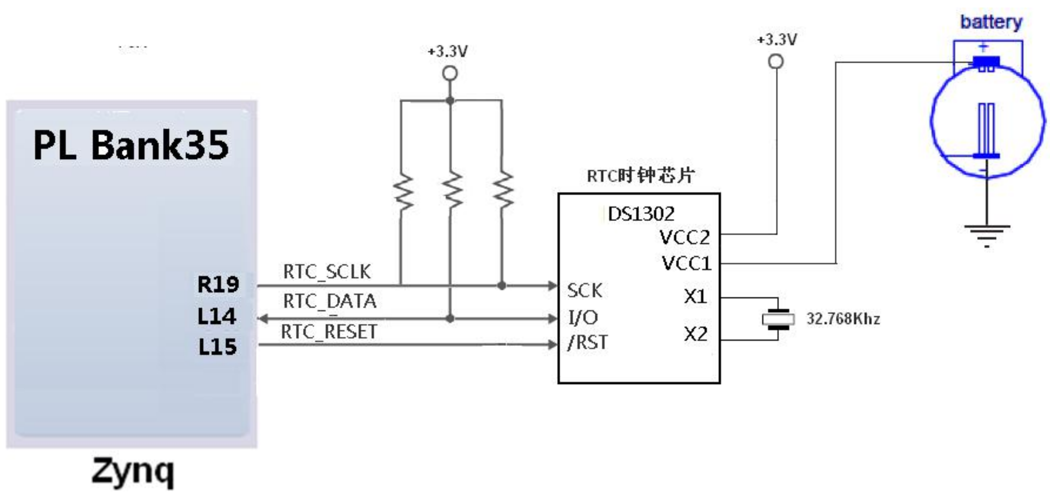


Figure 7-7: Real time clock DS1302 Schematic

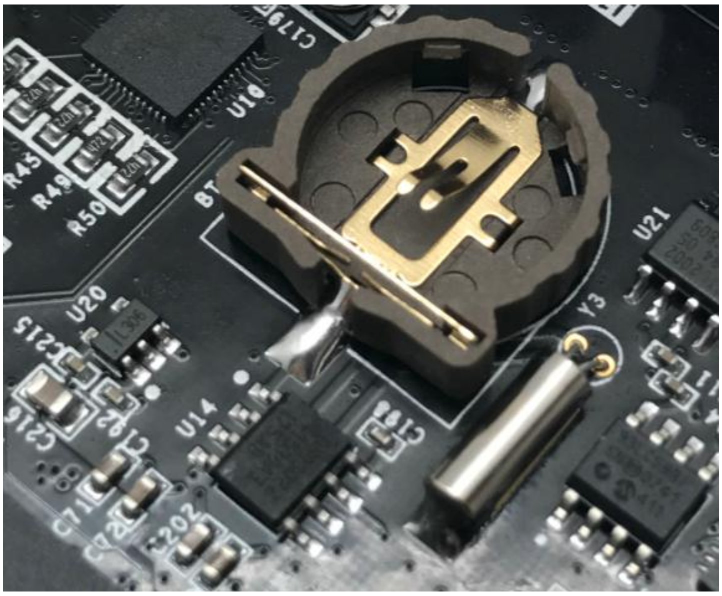


Figure 7-8: Real time clock DS1302 on the FPGA Board

Real Time Clock DSR1302 Pin Assignment

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
RTC _SCLK	**IO_0_34**	R19	RTC Clock Signal
RTC_RESET	**IO_L22N_T3_AD7N_35**	L15	RTC Reset Signal
RTC _DATA	**IO_L22P_T3_AD7P_35**	L14	RTC Data Signal

Part 7.4: Expansion Port J10

The expansion port J10 is a 40-pin 2.54mm double-row connector, which expands more peripherals and interfaces for users. Currently, the modules provided by ALINX include: ADDA module, LCD module, Gigabit Ethernet module, audio input/output module, matrix keyboard module, 500W binocular vision camera module, etc. The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channle ground and 34 IOs. The 34 IOs are connected to the BANK34 and BANK35 of ZYNQ PL. The default level is 3.3V. Parts of the 34IOs of the expansion port J10 can change the level by replacing the power chip (SPX3819M5-3-3) on the development board.

Do not directly connect the IO directly to the 5V device to avoid

burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. The P and N traces on the PCB design use differential traces to control the differential impedance to 100 ohms. The circuit of the expansion port (J10) is shown in Figure 7-9:

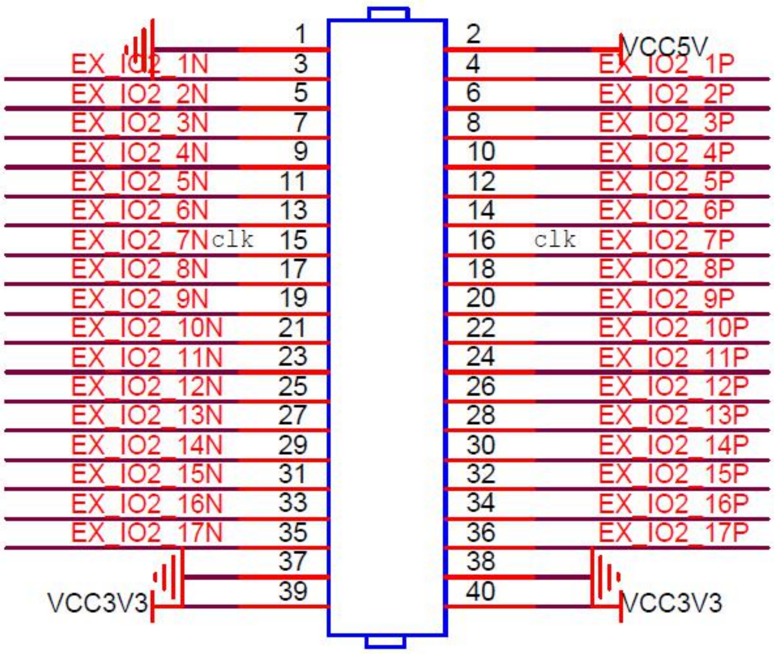


Figure 7-9: Expansion header J10 schematic

Figure 7-10 shows the physical diagram of the J10 expansion port. Pin1, Pin2 and Pin39 of the expansion port, Pin40 has been marked on the board.

Figure 7-10: Expansion header J10 on the FPGA Board

J10 Expansion Header Pin Assignment

J10 Pin	Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PIN1	GND	-	-
PIN2	+5V	-	-
PIN3	EX_IO1_1N	IO_L22N_T3_34	W19
PIN4	EX_IO1_1P	IO_L22P_T3_34	W18
PIN5	EX_IO1_2N	IO_L6N_T0_34	R14
PIN6	EX_IO1_2P	IO_L6P_T0_34	P14
PIN7	EX_IO1_3N	IO_L7N_T1_34	Y17
PIN8	EX_IO1_3P	IO_L7P_T1_34	Y16
PIN9	EX_IO1_4N	IO_L10N_T1_34	W15
PIN10	EX_IO1_4P	IO_L10P_T1_34	V15
PIN11	EX_IO1_5N	IO_L8N_T1_34	Y14
PIN12	EX_IO1_5P	IO_L8P_T1_34	W14
PIN13	EX_IO1_6N	IO_L23N_T3_34	P18
PIN14	EX_IO1_6P	IO_L23P_T3_34	N17
PIN15	EX_IO1_7N	IO_L11N_T1_34	U15
PIN16	EX_IO1_7P	IO_L11P_T1_34	U14
PIN17	EX_IO1_8N	IO_L24N_T3_34	P16
PIN18	EX_IO1_8P	IO_L24P_T3_34	P15
PIN19	EX_IO1_9N	IO_L9N _T1_34	U17
PIN20	EX_IO1_9P	IO_L9P_T1_34	T16
PIN21	EX_IO1_10N	IO_L21_N_T3_34	V18
PIN22	EX_IO1_10P	IO_L21_P_T3_34	V17
PIN23	EX_IO1_11N	IO_L5N_T0_34	T15
PIN24	EX_IO1_11P	IO_L5P_T0_34	T14
PIN25	EX_IO1_12N	IO_L3N_T0_34	V13
PIN26	EX_IO1_12P	IO_L3P_T0_34	U13
PIN27	EX_IO1_13N	IO_L4N_T0_34	W13
PIN28	EX_IO1_13P	IO_L4P_T0_34	V12
PIN29	EX_IO1_14N	IO_L2N_T0_34	U12
PIN30	EX_IO1_14P	IO_L2P_T0_34	T12
PIN31	EX_IO1_15N	IO_L1N_T0_34	T10
PIN32	EX_IO1_15P	IO_L1P_T0_34	T11
PIN33	EX_IO1_16N	IO_L2N_T0_35	A20
PIN34	EX_IO1_16P	IO_L2P_T0_35	B19
PIN35	EX_IO1_17N	IO_L1N_T0_35	B20

PIN36	EX_IO1_17P	IO_L1P_T0_35	C20
PIN37	GND	-	-
PIN38	GND	-	-
PIN39	+3.3V	-	-
PIN40	+3.3V	-	-

Part 7.5: Expansion Port J11

The expansion port J10 is a 40-pin 2.54mm double-row connector, which expands more peripherals and interfaces for users. Currently, the modules provided by ALINX include: ADDA module, LCD module, Gigabit Ethernet module, audio input/output module, matrix keyboard module, 500W binocular vision camera module, etc. The expansion port has 40 signals, of which 1-channel 5V power supply, 2-channel 3.3 V power supply, 3-channnle ground and 34 IOs. The 34 IOs are connected to the BANK35 ZYNQ PL. The default level is 3.3V. All the 34IOs of the expansion port J11 can change the level by replacing the power chip (SPX3819M5-3-3) on the development board.

Do not directly connect the IO directly to the 5V device to avoid burning the FPGA. If you want to connect 5V equipment, you need to connect level conversion chip.

A 33 ohm resistor is connected in series between the expansion port and the FPGA connection to protect the FPGA from external voltage or current. The P and N traces on the PCB design use differential traces to control the differential impedance to 100 ohms. The circuit of the expansion port (J11) is shown in Figure 7-11:

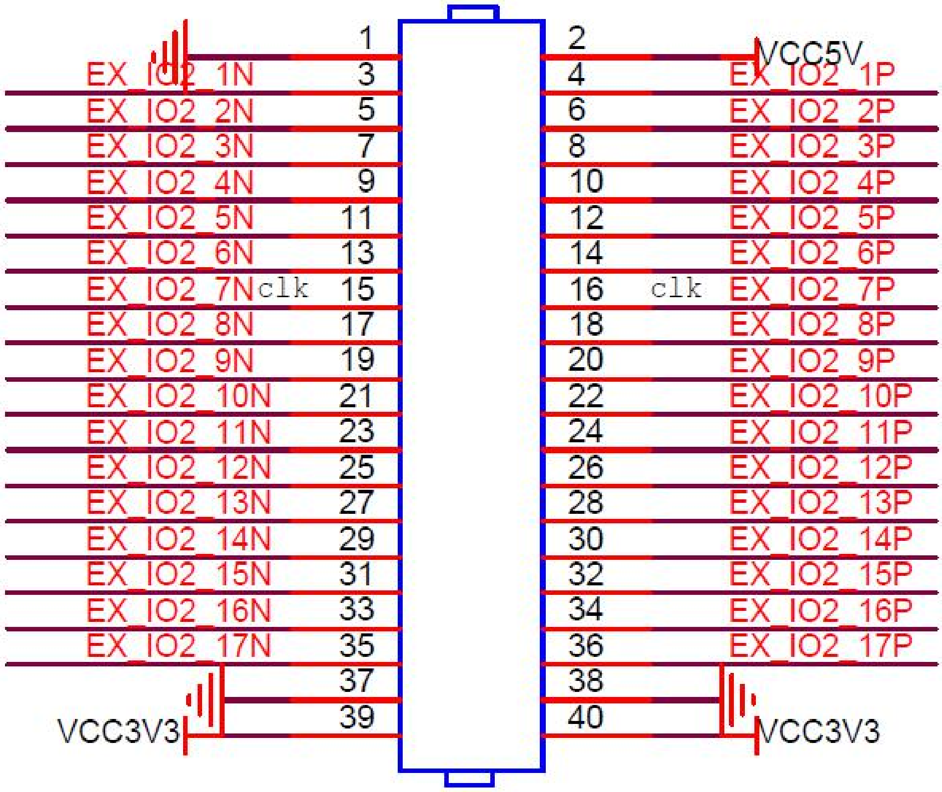


Figure 7-11: Expansion header J11 schematic

Figure 7-12 shows the physical diagram of the J11 expansion port. Pin1, Pin2 and Pin39 of the expansion port, Pin40 has been marked on the board.

Figure 7-12: Expansion header J11 on the FPGA Board

J11 Expansion Header Pin Assignment

J11 Pin	Signal Name	ZYNQ Pin Name	ZYNQ Pin Number
PIN1	GND	-	-
PIN2	+5V	-	-
PIN3	EX_IO2_1N	IO_L6N_T0_35	F17
PIN4	EX_IO2_1P	IO_L6P_T0_35	F16
PIN5	EX_IO2_2N	IO_L15N_T2_35	F20
PIN6	EX_IO2_2P	IO_L15P_T2_35	F19
PIN7	EX_IO2_3N	IO_L18N_T2_35	G20
PIN8	EX_IO2_3P	IO_L18P_T2_35	G19
PIN9	EX_IO2_4N	IO_L14N_T2_35	H18
PIN10	EX_IO2_4P	IO_L14P_T2_35	J18
PIN11	EX_IO2_5N	IO_L9N_T1_35	L20
PIN12	EX_IO2_5P	IO_L9P_T1_35	L19
PIN13	EX_IO2_6N	IO_L7N_T1_35	M20
PIN14	EX_IO2_6P	IO_L7P_T1_35	M19
PIN15	EX_IO2_7N	IO_L12N_T1_35	K18
PIN16	EX_IO2_7P	IO_L12P_T1_35	K17
PIN17	EX_IO2_8N	IO_L10N_T1_35	J19
PIN18	EX_IO2_8P	IO_L10P_T1_35	K19
PIN19	EX_IO2_9N	IO_L17N_T2_35	H20
PIN20	EX_IO2_9P	IO_L17P_T2_35	J20
PIN21	EX_IO2_10N	IO_L11N_T1_35	L17
PIN22	EX_IO2_10P	IO_L11P_T1_35	L16
PIN23	EX_IO2_11N	IO_L8N_T1_35	M18
PIN24	EX_IO2_11P	IO_L8P_T1_35	M17
PIN25	EX_IO2_12N	IO_L4N_T0_35	D20
PIN26	EX_IO2_12P	IO_L4P_T0_35	D19
PIN27	EX_IO2_13N	IO_L5N_T0_35	E19
PIN28	EX_IO2_13P	IO_L5P_T0_35	E18
PIN29	EX_IO2_14N	IO_L16N_T2_35	G18
PIN30	EX_IO2_14P	IO_L16P_T2_35	G17
PIN31	EX_IO2_15N	IO_L13N_T2_35	H17
PIN32	EX_IO2_15P	IO_L13P_T2_35	H16

PIN33	EX_IO2_16N	IO_L19N_T3_35	G15
PIN34	EX_IO2_16P	IO_L19P_T3_35	H15
PIN35	EX_IO2_17N	IO_L20N_T3_35	J14
PIN36	EX_IO2_17P	IO_L20P_T3_35	K14
PIN37	GND	-	-
PIN38	GND	-	-
PIN39	+3.3V	-	-
PIN40	+3.3V	-	-

Part 7.6: User LEDs

On the AX7010 FPGA development board, four LEDs are connected to the BANK35 IO in the PL section, When the BANK35 IO voltage is high, the LED light is off, and when the BANK35 IO voltage is low, the LED will be illuminated. A schematic diagram of the ZYNQ BANK35 IO and LEDs connections is shown in Figure 7-13:

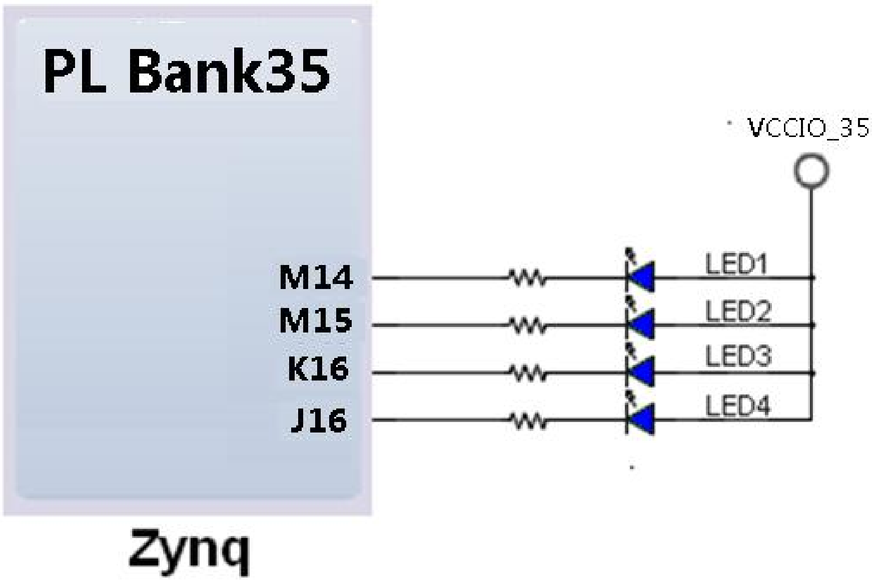


Figure 7-13: PL User LEDs Schematic

Figure 7-14: PL User LEDs on the FPGA Board

PL User LEDs pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
LED1	IO_L23P_T3_35	M14	PL User LED PL LED1
LED2	IO_L23N_T3_35	M15	PL User LED PL LED2
LED3	IO_L24P_T3_35	K16	PL User LED PL LED3
LED4	IO_L24N_T3_35	J16	PL User LED PL LED4

Part 7.7: User Buttons

On the AX7010 development board, four user buttons are connected to the IOs of BANK34 and Bank35 in the ZYNQ PL section. The buttons are active low. In the circuit design, when the button is pressed, the signal is low, and when it is not pressed, the signal is high. The schematic is shown in Figure 7-15:

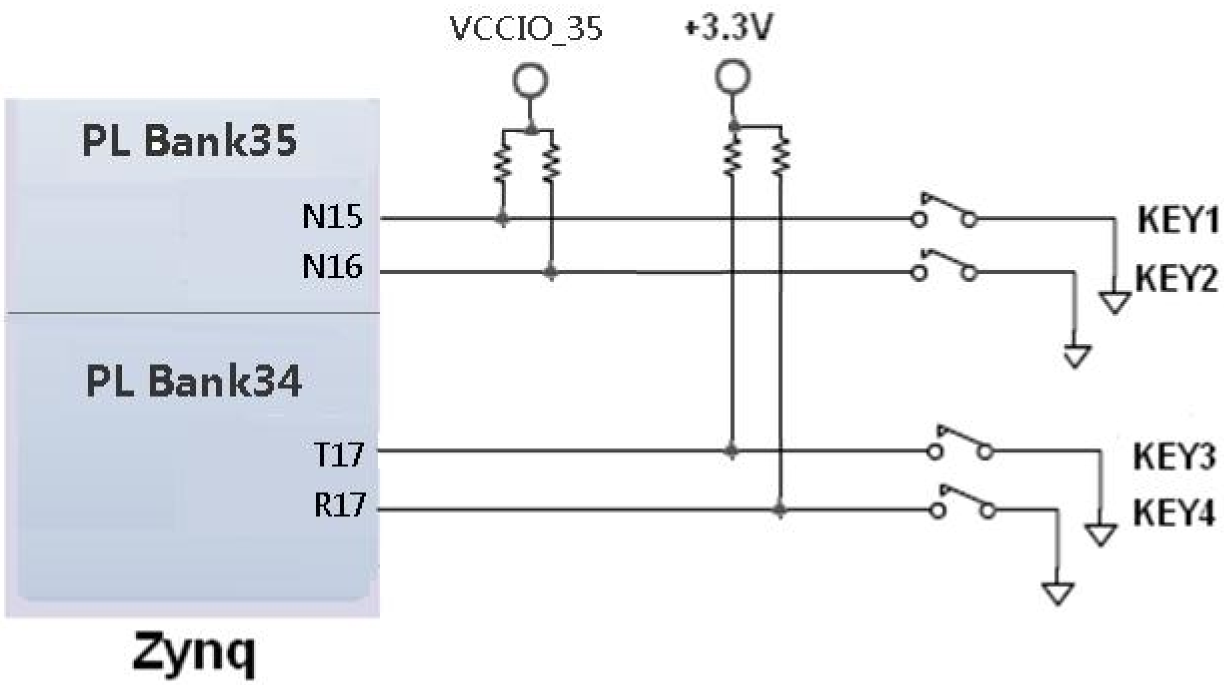


Figure 7-15: PL User Buttons Schematic

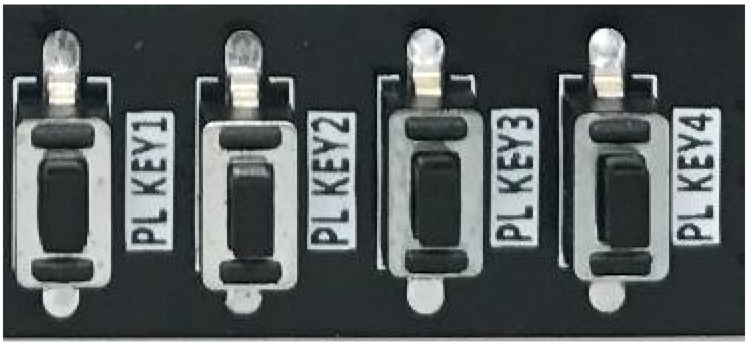


Figure 7-16: PL User Buttons on the FPGA Board

PL User LEDs pin assignment:

Signal Name	ZYNQ Pin Name	ZYNQ Pin Number	Description
KEY1	IO_L21P_T3_35	N15	PL User Button PL KEY1
KEY2	IO_L21P_T3_35	N16	PL User Button PL KEY2
KEY3	IO_L20P_T3_34	T17	PL User Button PL KEY3
KEY4	IO_L19N_T3_34	R17	PL User Button PL KEY4