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Flaircomm Technologies Inc.

FLC-BTM402/FLC-BTMDC747 Datasheet

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1. Introduction

FLC-BTM402/FLC-BTMDC747 is a small form factor, low power and highly economic Bluetooth radio module that allows OEM to add wireless capability to their products. The module supports multiple interfaces that make it simple to design into fully certified embedded Bluetooth solutions.

With FLC's AT+ programming interfaces, designers can easily customize their applications to support different Bluetooth profiles, such as SPP, DUN, HDP, and etc. The module supports Bluetooth® Enhanced Data Rate (EDR) and delivers up to 3 Mbps data rate for distances to 10M.

The module is an appropriate product for designers who want to add wireless capability to their products.

1.1 Naming Declaration

New Naming	Old Naming
FLC-BTM402	FLC-BTMDC747

Table 1: Naming Declaration

1.2 Block Diagram

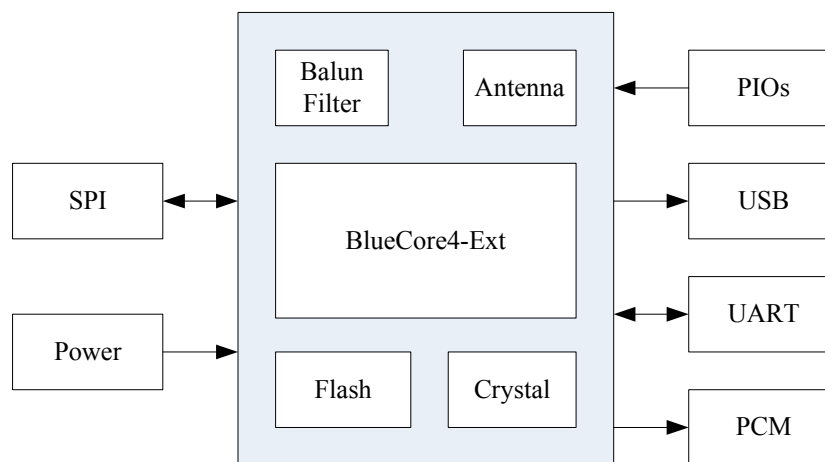


Figure 1: Block Diagram

1.3 Features

- Bluetooth v2.1+EDR, Class 2
- On-board antenna design
- UART and USB programming and data interfaces



- PCM digital audio interface
- 8MB on board flash
- Small form factor
- SMT pads for easy and reliable PCB mounting
- BQB/FCC/CE Certified
- RoHS compliant

1.4 Applications

- Cable replacement
- Bar code and RFID scanners
- Measurement and monitoring systems
- Industrial sensors and controls
- Medical devices
- Industrial PCs and laptops

2. General Specification

Bluetooth Specification	
Standard	Bluetooth2.1+EDR, Class II
Profiles	SPP, DUN, HDP, etc. detailed profiles depends on the firmware
Frequency Band	2.402G ~ 2.480G
Maximum Data Rate	3Mbps
Antenna	On-Board
Baseband Crystal OSC	16MHz
Interface	UART, PIO, AIO, USB, SPI, PCM
Sensitivity	-84dBm@0.1%BER
RF TX Power	4dBm
Power	
Supply Voltage	2.7 ~ 3.6V DC
Working Current	Depends on profiles, 30mA typical
Standby Current	<1mA
Operating Environment	
Temperature	-20°C to +70°C
Humidity	10%~90% Non-Condensing
Certifications	BQB/FCC/CE
Environmental	RoHS Compliant
Dimension and Weight	
Dimension	13.40mm x 25.80mm x 2.40mm
Weight	1.5g

Table 2: General Specification

3. Pin Definition

3.1 Pin Configuration

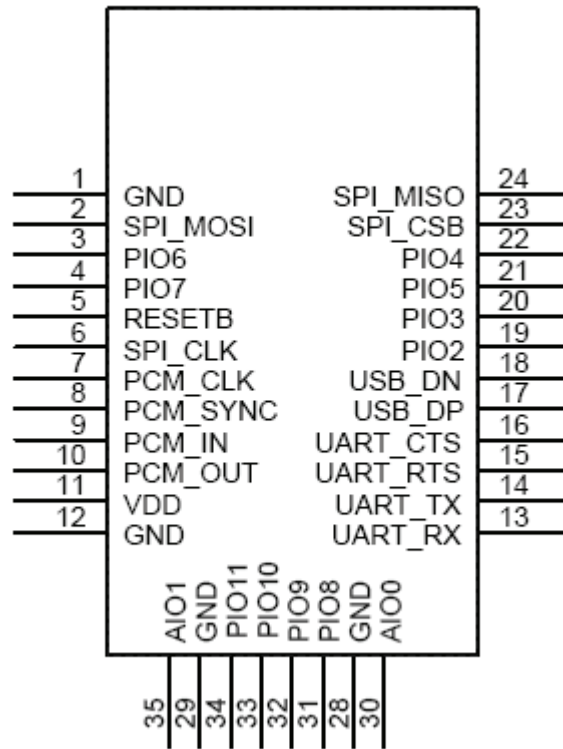


Figure 2: Pin Configuration

3.2 Pin Definition

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	SPI_MOSI	CMOS input with weak internal pull-down	Serial Peripheral interface data input. Programming only.
3	PIO6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
4	PIO7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
5	RESETB	CMOS input with weak internal pull-up	Active LOW reset.
6	SPI_CLK	CMOS input with weak internal pull-down	Serial Peripheral interface clock. Programming only.
7	PCM_CLK	Bi-directional with weak	PCM interface, synchronous data clock. No



		internal pull-down	connect if not use.
8	PCM_SYNC	Bi-directional with weak internal pull-down	PCM interface, synchronous data sync. No connect if not use.
9	PCM_IN	CMOS input with weak internal pull-down	PCM interface, synchronous data input. No connect if not use.
10	PCM_OUT	CMOS output, tri-state, with weak internal pull-down	PCM interface, synchronous data output. No connect if not use.
11	VDD	Power	3.3V regulated power supply
12	GND	Ground	Ground
13	UART_RX	CMOS input with weak internal pull-down	UART receive data input
14	UART_TX	CMOS output, tri-state, with weak internal pull-up	UART transmit data output
15	UART_RTS	CMOS output, tri-state, with weak internal pull-up	UART request to send, active low, set HIGH to disable host transmitter
16	UART_CTS	CMOS input with weak internal pull-down	UART Clear to send, active low, if set HIGH, disables transmitter
17	USB_DP	Bi-directional	USB data plus. Pull up 1.5K when active
18	USB_DN	Bi-directional	USB data minus.
19	PIO2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
20	PIO3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
21	PIO5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
22	PIO4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
23	SPI_CSB	CMOS input with weak internal pull-up	Chip select for synchronous serial interface, active low. Programming only.
24	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral interface data output. Programming only.
28	GND	Ground	Ground
29	GND	Ground	Ground
30	AIO0	Bi-directional	Programmable analog input/output
31	PIO8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
32	PIO9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
33	PIO10	Bi-directional with programmable	Programmable input/output



		strength internal pull-up/down	
34	PIO11	Bi-directional with programmable strength internal pull-up/down	Programmable input/output
35	AIO1	Bi-directional	Programmable analog input/output

Table 3: Pin Definition

4. Physical Interfaces

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less. It is essential that the power rail recovers quickly.

4.2 Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via a software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The PIOs have weak pull-downs.

Pin Name / Group	Pin Status on Reset
USB_DP	Input with PD
USB_DN	Input with PD
UART_RX	Input with PD
UART_CTS	Input with PD
UART_TX	Tri-state output with PU
UART_RTS	Tri-state output with PU
SPI_MOSI	Input with PD
SPI_CLK	Input with PD
SPI_CSB	Input with PU
SPI_MISO	Tri-state output with PD
PCM_CLK	input with PD
PCM_SYNC	input with PD
PCM_IN	input with PD
PCM_OUT	Tri-state with PD
RESET	Input with PU
PIOs	Bi-directional with PU/PD
AIOs	Output, drive low
RF-IN	High impedance

Table 4: Pin Status on Reset

Note: Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

4.3 Digital Audio Interfaces

The module has offered PCM digital audio interface.

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, the module has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for applications. The module offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on the module allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

The module can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. The module is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ -law or A-law companded sample formats at 8k samples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

The module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channels A-law and μ -law CODEC
- Motorola MC145481 8-bit A-law and μ -law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs

The module is also compatible with the Motorola SSI™ interface.

4.3.1 PCM Interface Master/Slave

When PCM is configured as a master, the module generates PCM_CLK and PCM_SYNC.

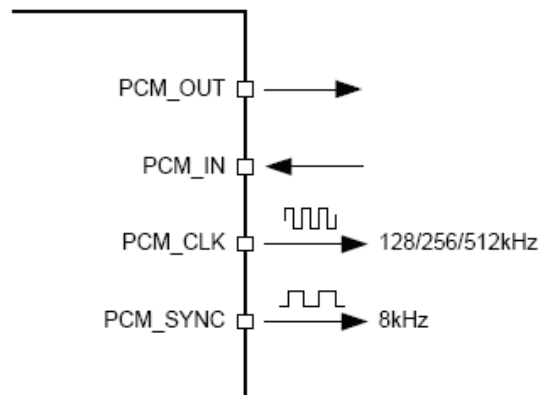


Figure 3: Configured PCM as a Master

When PCM is configured as the slave, the module accepts PCM_CLK rates up to 2048kHz.

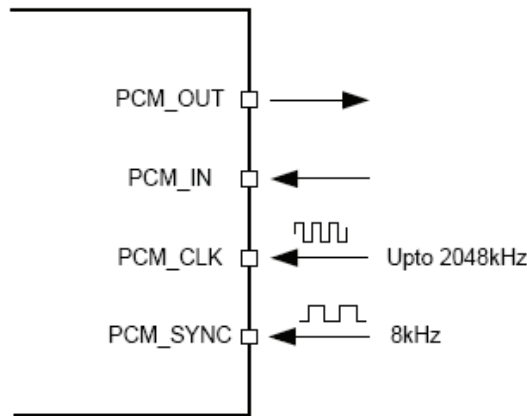


Figure 4: Configured PCM as a Slave

4.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When the module is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When the module is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5μs long.

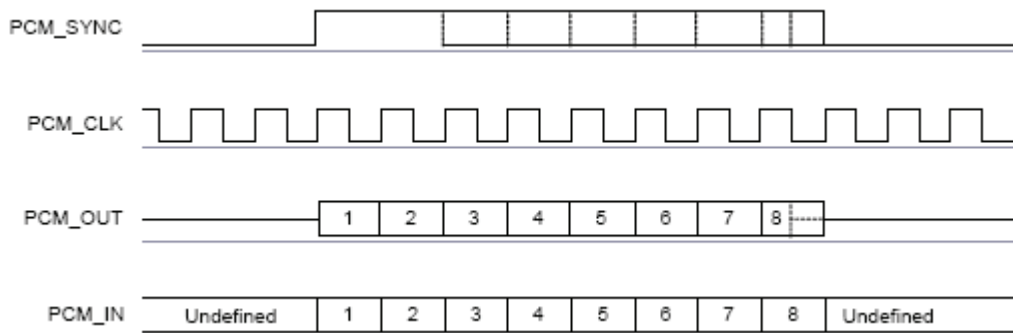


Figure 5: Long Frame Sync (Shown with 8-bit Companded Sample)

4.3.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

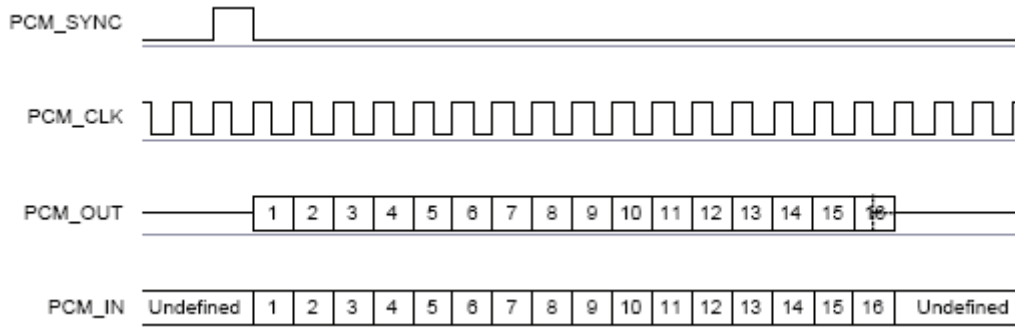


Figure 6: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, the module samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

4.3.4 Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

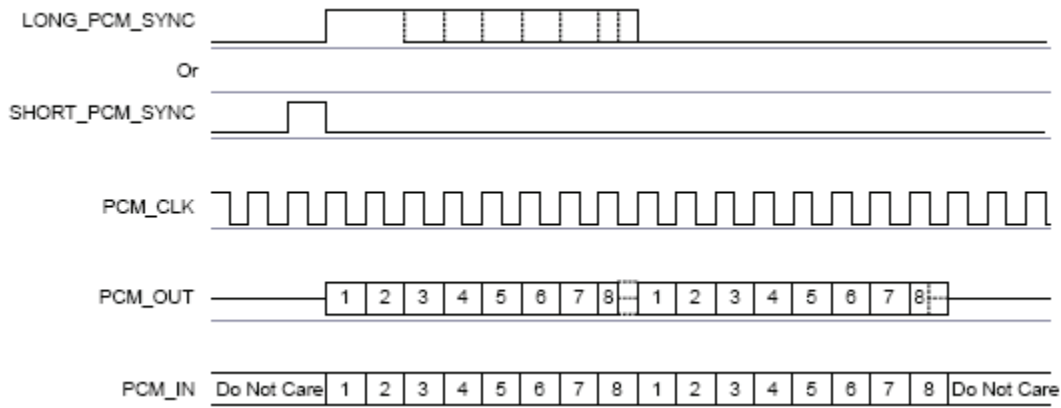


Figure 7: Multi-Slot Operation with Two Slots and 8-bit Companded Samples

4.3.5 GCI Interface

The module is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

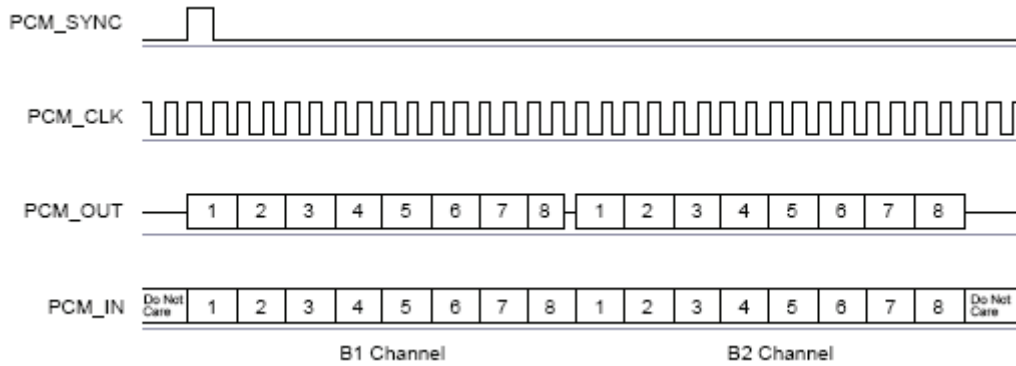


Figure 8: GCI Interface

The start of a frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With the module in slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

4.3.6 Slots and Sample Formats

The module can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats. The module supports 13-bit linear, 16-bit linear and 8-bit μ -law or A-law sample formats. The sample rate is 8k samples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

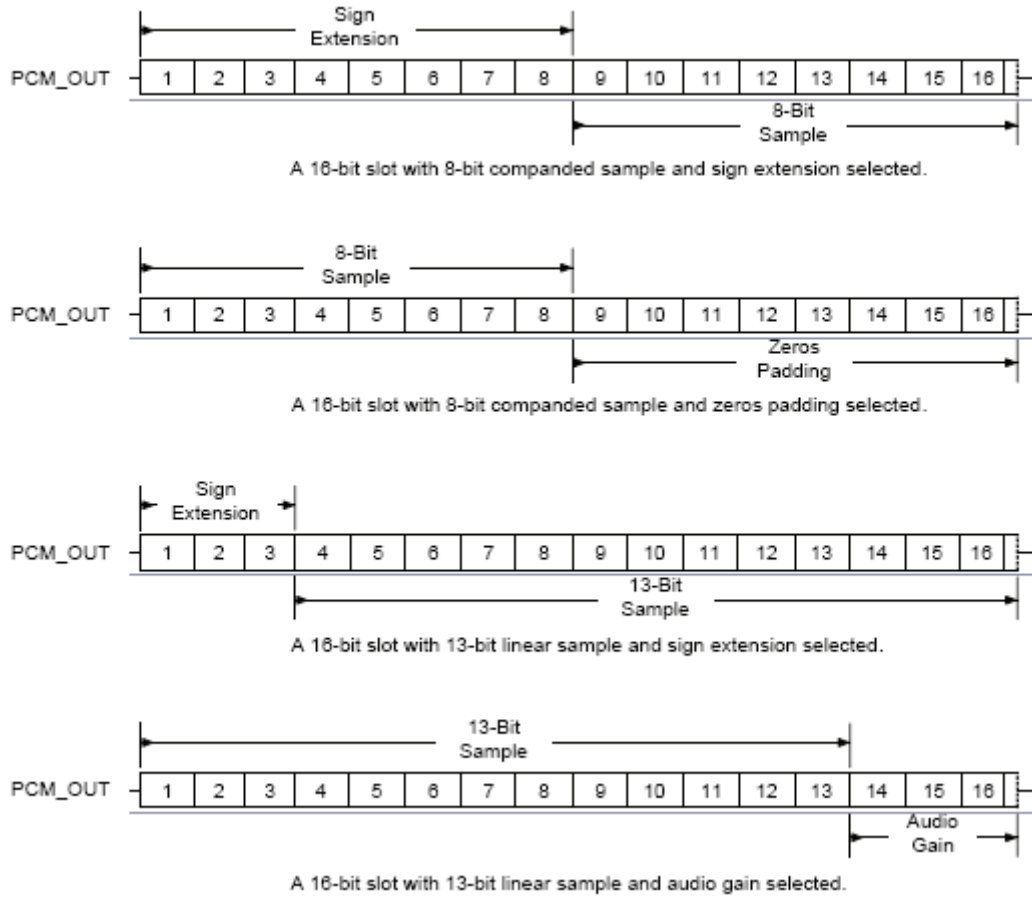


Figure 9: 16-Bit Slot Length and Sample Formats

4.3.7 Additional Features

The module has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

4.3.8 PCM Timing Information

Symbol	Parameter		Min	Typical	Max	Unit
fmclk	PCL_CLK Frequency	4MHz DDS generation. Selection of frequency is programmable.	-	128	-	kHz
				256		
				512		

		48MHz DDS generation. Selection of frequency is programmable.	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
tmclk ^(a)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
tmckl ^(a)	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
tdmclksynch	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
tdmclkpout	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
tdmcklsynch	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
tdmckhsynch	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
tdmcklpoutz	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
tdmckhpoutz	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
tsupinckl	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
thpinckl	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 5: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

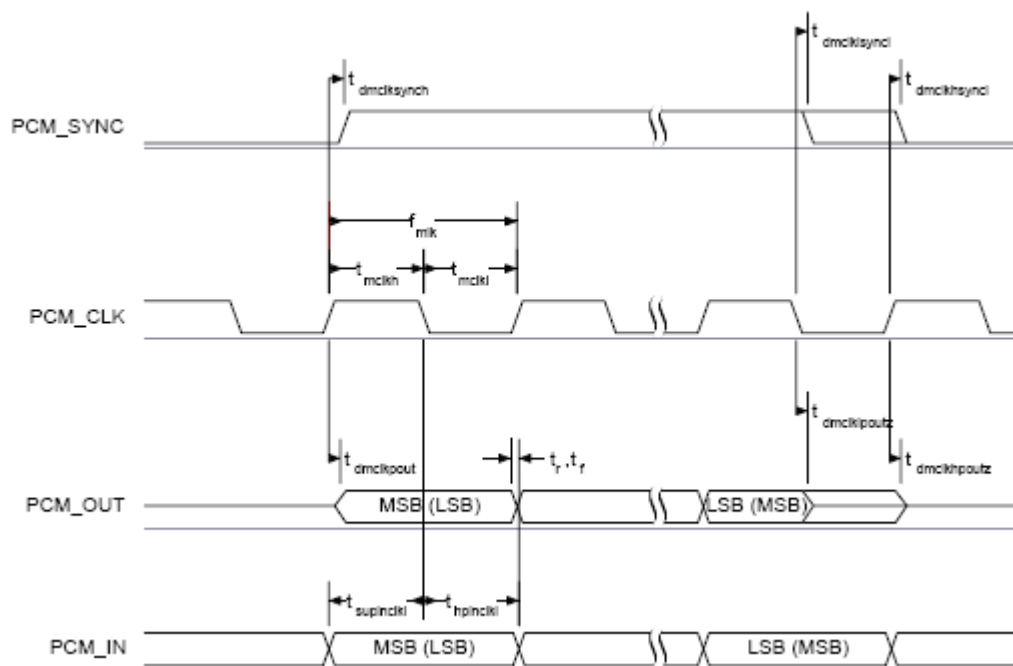


Figure 10: PCM Master Timing Long Frame Sync

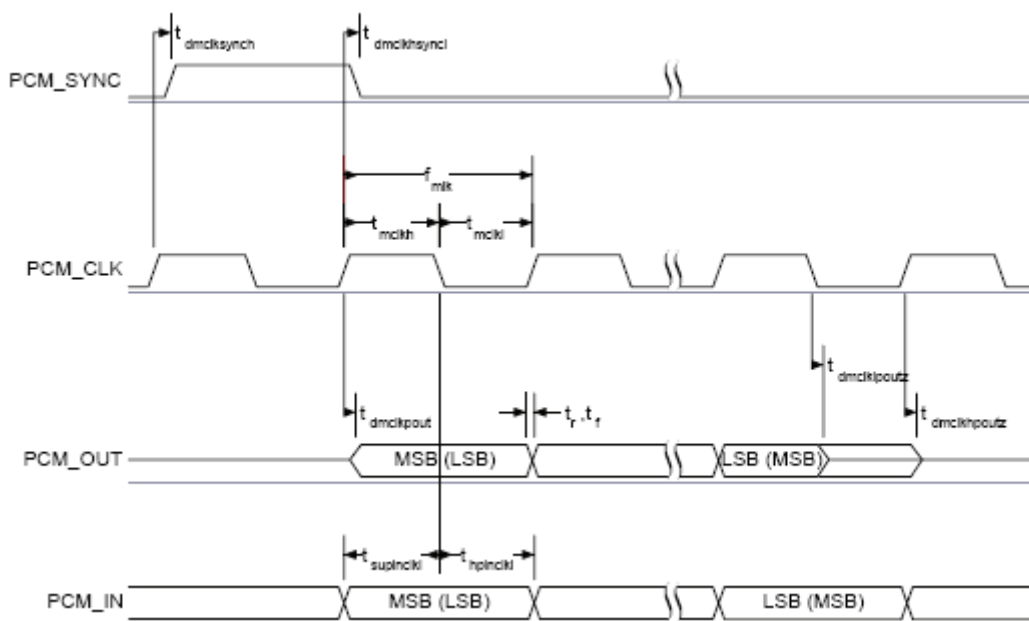


Figure 11: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typical	Max	Unit
fclk	PCM clock frequency (Slave mode: input)	64	-	2048	kHz
fclk	PCM clock frequency (GCI mode)	128	-	4096	kHz



tscclk	PCM_CLK low time	200	-	-	ns
tscclkh	PCM_CLK high time	200	-	-	ns
thscclksynch	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
tsusclksynch	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
tdpout	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
tdscclkhout	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
tdpoutz	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
tsupinsckl	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
thpinsckl	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 6: PCM Slave Timing

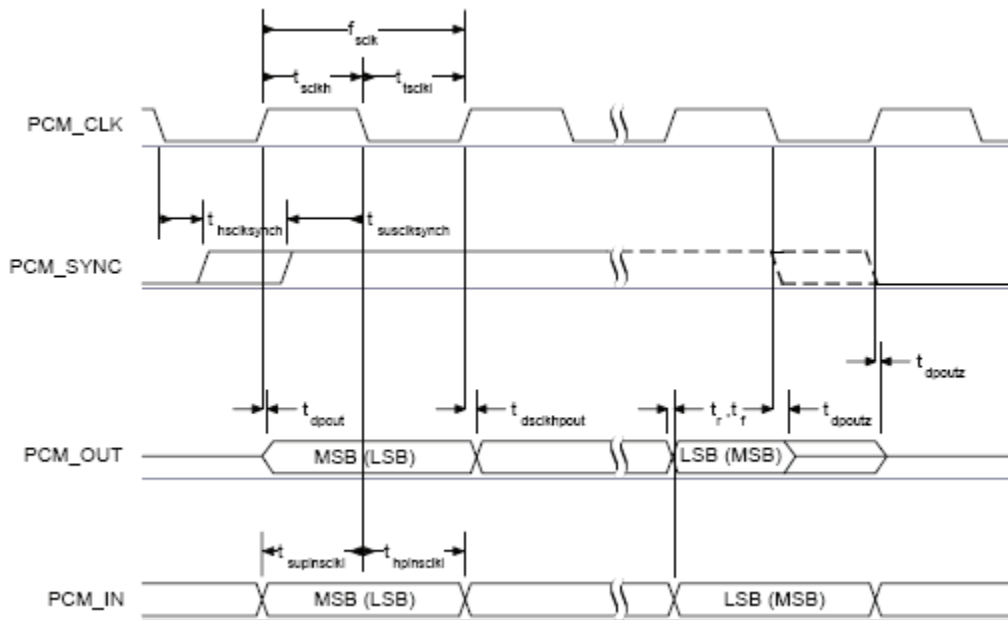


Figure 12: PCM Slave Timing Long Frame Sync

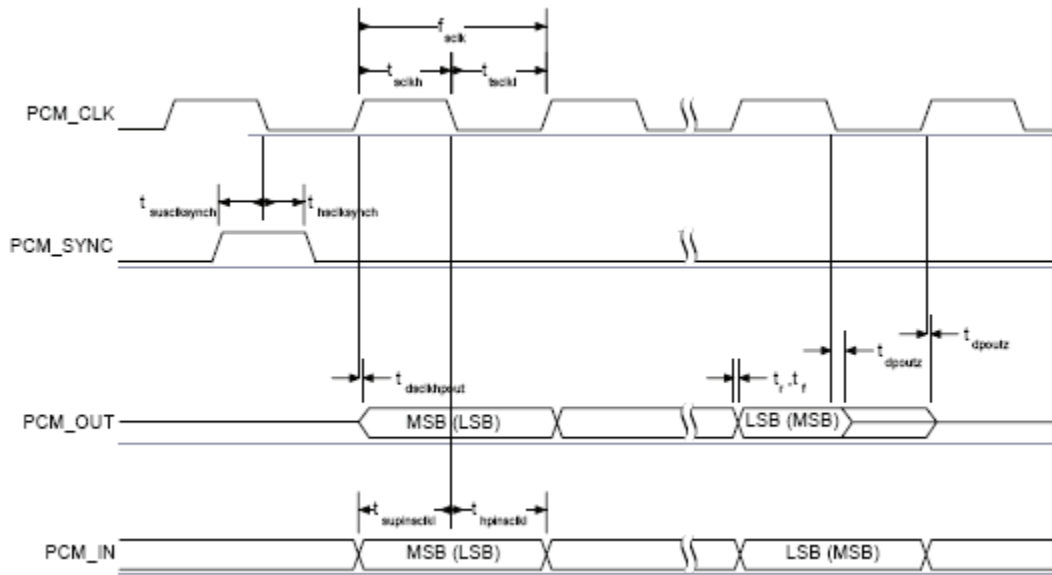


Figure 13: PCM Master Timing Short Frame Sync

4.4 RF Interface

The module has a built-in high performance antenna.

4.5 General Purpose Analogue IO

The general purpose analog IOs can be configured as ADC inputs by software. Do not connect them if not use.

4.6 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

4.7 Serial Interfaces

4.7.1 UART

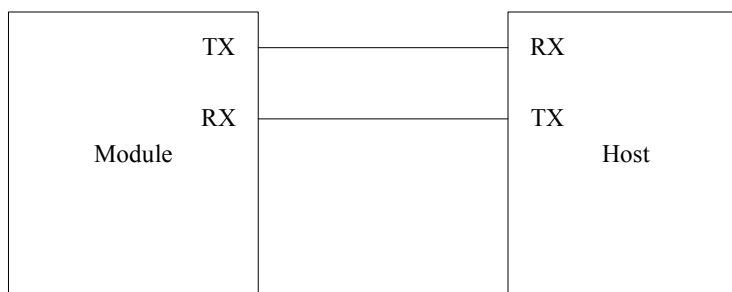
This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators. PIO10 and PIO11 can be configured as UART_DTR and UART_RTS.

Parameter		Possible Values
Baud Rate	Minimum	1200 baud ($\leq 2\%$ Error)
		9600 baud ($\leq 1\%$ Error)
	Maximum	3M baud ($\leq 1\%$ Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

Table 7: Possible UART Settings

When connecting the module to a host, please make sure to follow **Figure 14**.


Figure 14: UART Connection

4.7.2 USB

There is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller such as PC.

The module features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device. The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a $15k\Omega \pm 5\%$ pull-down resistor (in the hub/host) when $VDD = 3.1V$. This presents a Thevenin resistance to the host of at least 900Ω . Alternatively, an external $1.5k\Omega$ pull-up resistor can be placed between a PIO line and DP on the USB cable.

4.7.2.1 Self-Powered Mode

In self-powered mode, the module is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to module via a resistor network (Rvb1 and Rvb2), so the module can detect when VBUS is powered up. The module will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or LDO) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5K Ω 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The internal pull-up in the module is only suitable for bus-powered USB devices, e.g., dongles.

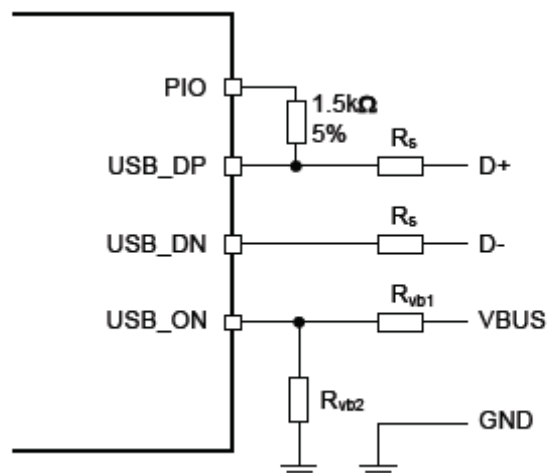


Figure 15: USB Connections for Self-Powered Mode

Note:

USB_ON is shared with the module PIO terminals.

Identifier	Value	Function
R _s	27 Ω Nominal	Impedance matching to USB cable
R _{vb1}	22k Ω 5%	VBUS ON sense divider
R _{vb2}	47k Ω 5%	VBUS ON sense divider

Table 8: USB Interface Component Values

4.7.2.2 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. The module negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume. For Class 2 Bluetooth applications, FLC recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, the module requests 100mA during enumeration. For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA. When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See USB Specification v1.1, section 7.2.4.1. Some applications may require soft start circuitry to limit inrush current if more than 10 μ F is present between VBUS and GND.

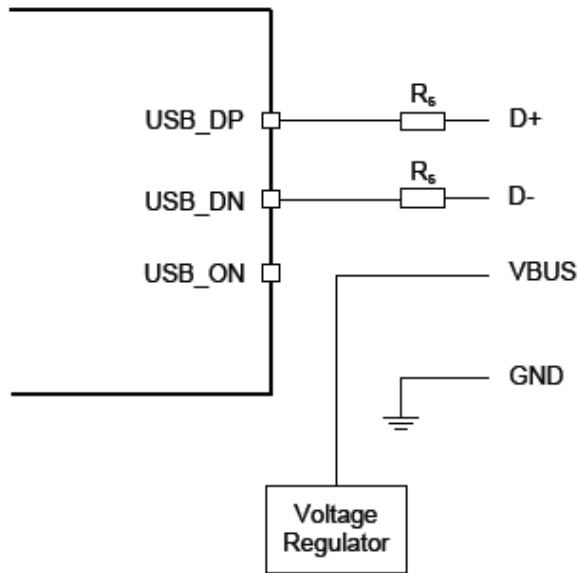


Figure 16: USB Connections for Bus-Powered Mode

4.7.3 I²C

PIO[8:6] can be used to form a master I²C interface. The interface is formed using software to drive these lines. It is suited only to relatively slow functions such as driving a LCD, Keyboard, scanner or EEPROM. In the case, PIO lines need to be pulled up through 2.2Kohm resistors.

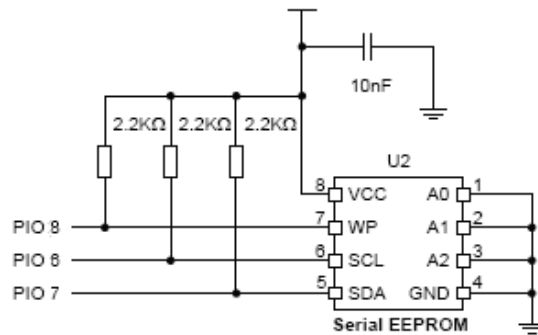


Figure 17: Example EEPROM Connection with I²C Interface

4.7.4 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins. Testing points for the SPI interface are reserved on board in case that the firmware shall be updated during manufacture.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is



running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

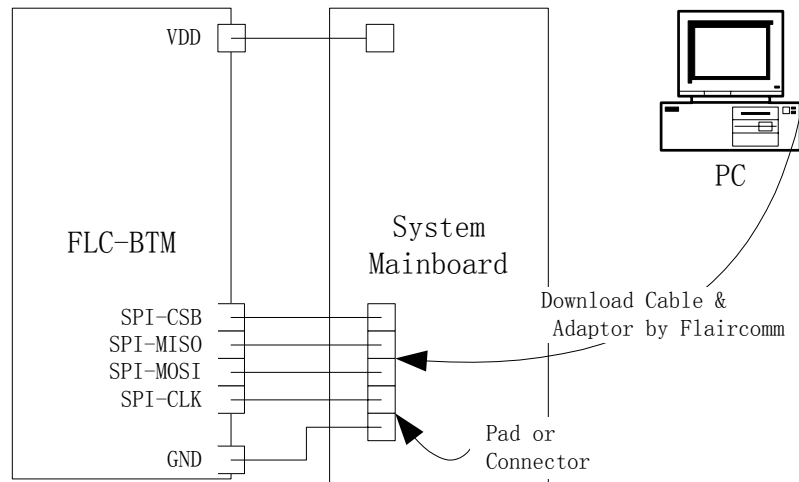


Figure 18: Design SPI for In-System Programming

5. Electrical Characteristic

5.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+120	°C
Operating Temperature	-40	+85	°C
PIO/AIO Voltage	-0.4	+3.6	V
VDD	-0.4	+3.7	V
USB_DP/USB_DN Voltage	-0.4	+3.6	V
Other Terminal Voltages except RF	-0.4	VDD+0.4	V

Table 9: Absolute Maximum Rating

5.2 Recommended Operating Conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	--	+85	°C
Operating Temperature Range	-20	--	+70	°C
VDD	+2.7	+3.3	+3.6	V

Table 10: Recommended Operating Conditions

5.3 Input/output Terminal Characteristics

5.3.1 Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
VIL input logic level low	-0.4	-	+0.8	V
VIH input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage Levels				
V _{OL} output logic level low, I _{OL} = 4.0mA	-	-	0.4	V
V _{OH} output logic level high, I _{OH} = -4.0mA	VDD-0.2	-	-	V
Input and Tri-state Current				
With strong pull-up	-100	-40	-10	μA
With strong pull-down	10	40	100	μA
With weak pull-up	-5	-1.0	-0.2	μA
With weak pull-down	-0.2	+1.0	5.0	μA

I/O pad leakage current	-1	0	+1	μA
CI Input Capacitance	1.0	-	5.0	pF

Table 11: Digital Terminal

5.3.2 USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
V _{IL} input logic level low	-	-	0.3VDD	V
V _{IH} input logic level high	0.7VDD	-	-	V
Input Leakage Current				
GND < V _{IN} < VDD ^(a)	-1	1	5	μA
CI Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V _{IL} output logic level low	0.0	-	0.2	V
V _{IH} output logic level high	2.8	-	VDD	V

Table 12: USB Terminal

(a) Internal USB pull-up disabled

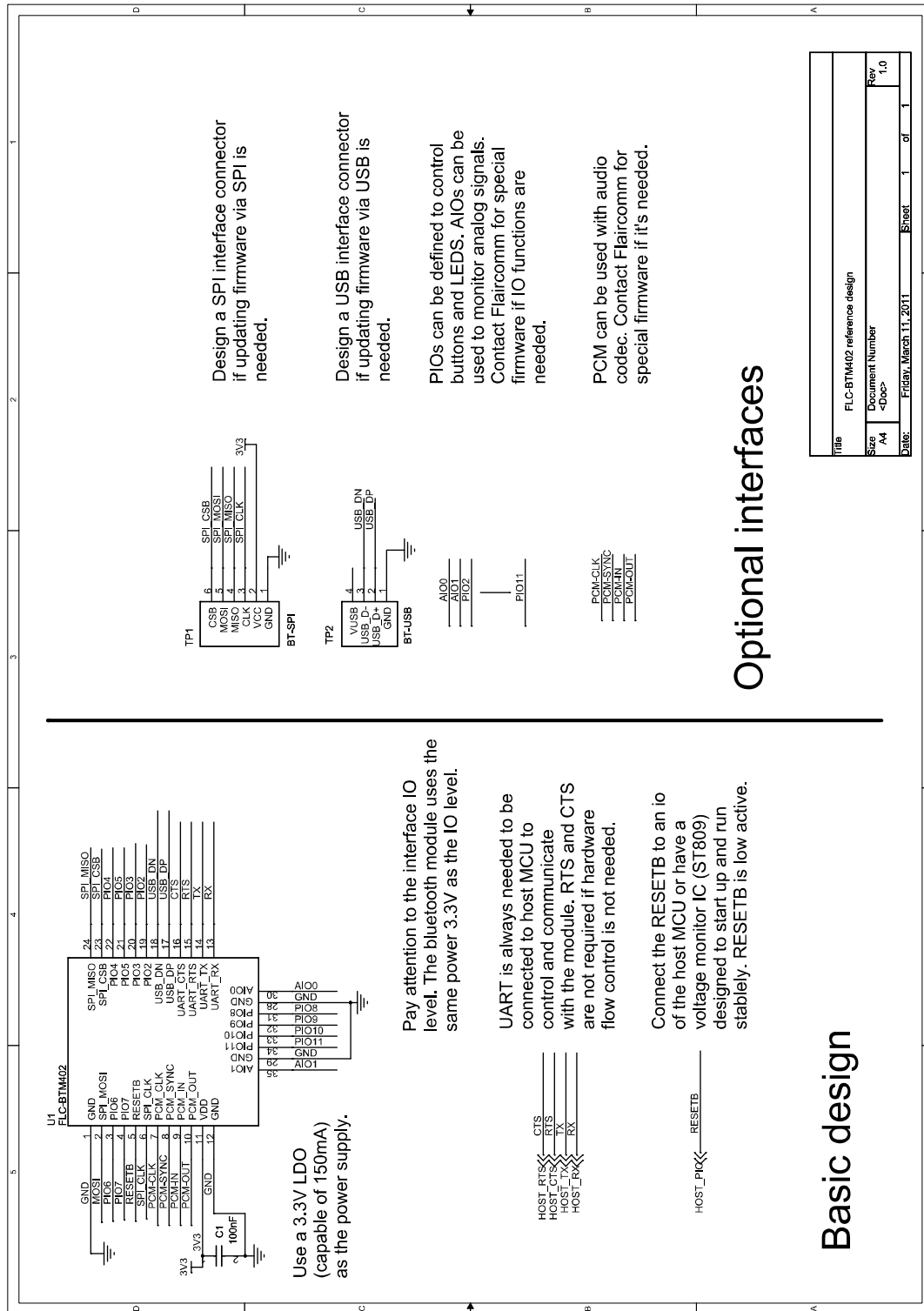
5.4 Power consumptions

Operating Condition	Min	Typical	Max	Unit
Radio On* (Discovery or Inquiry window time)		40		mA
Connected Idle (No Sniff)		25		mA
Connected Idle (Sniff 100 milli secs)		12		mA
Connected with data transfer	40	45	50	mA
Deep Sleep Idle mode		26		uA

Table 13: Power consumptions

Note: If the module is in SLAVE mode, the bursts of the radio ON time will vary with the windows. The average current depends on how the windows being set.

6. Reference Design



7. Mechanical Characteristic

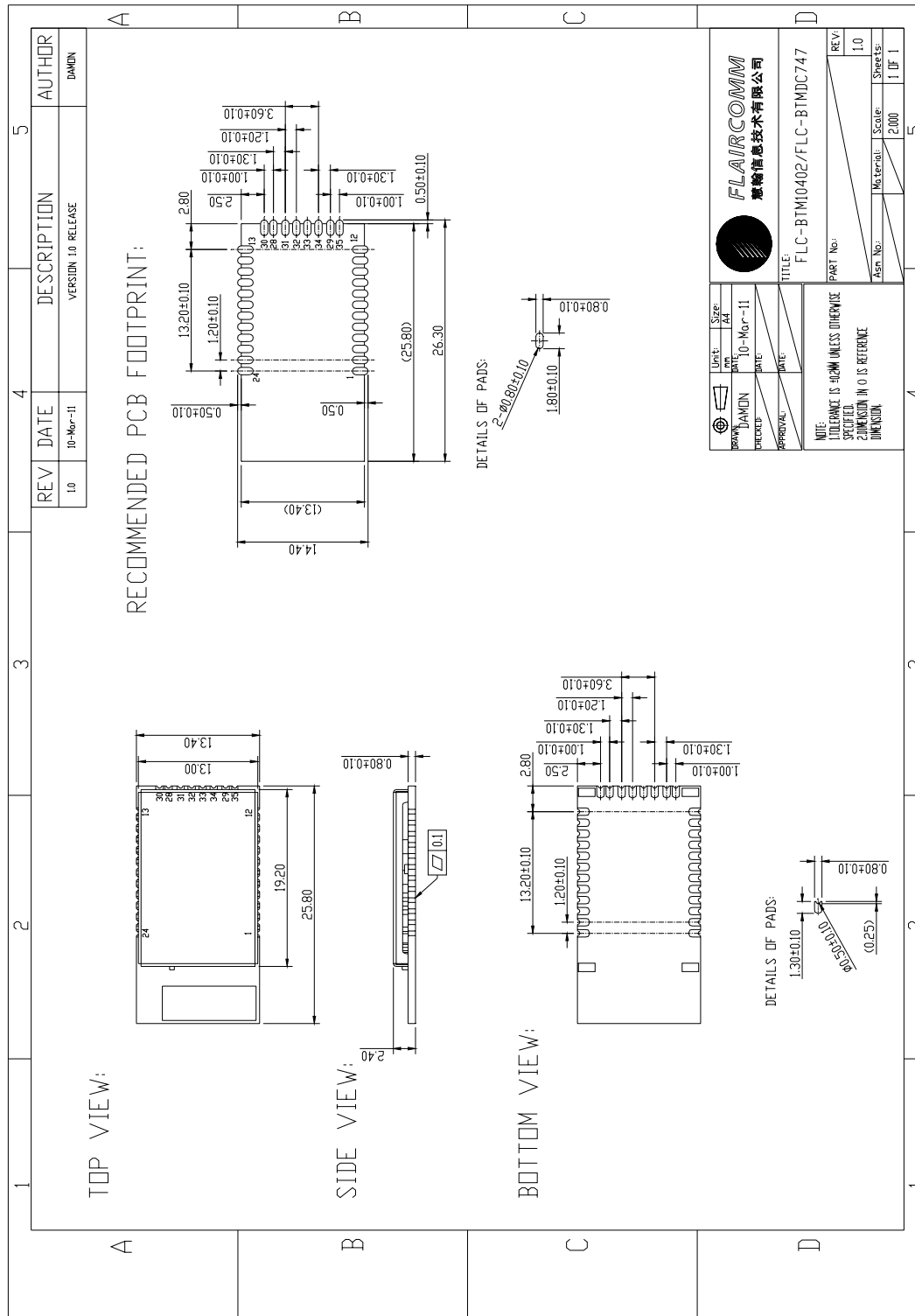


Figure 20: Mechanical Characteristic

8. Recommended PCB Layout and Mounting Pattern

A very important factor in achieving maximum Bluetooth performance is the placement of a module with on-board antenna designs onto the carrier board and corresponding PCB layout. There should be no any trace, ground and vias in the area of the carrier board underneath the module's on-board antenna section as indicated in **Figure 21**. Antenna portion of the module must be placed at least 5mm away from any metal part and the antenna should not be covered by any piece of metal. The antenna of the module **MUST** be kept as far from potential noise sources as possible and special care must also be taken with placing the module in proximity to circuitry that can emit heat. The RF part of the module is very sensitive to temperature and sudden changes can have an adverse impact on performance.

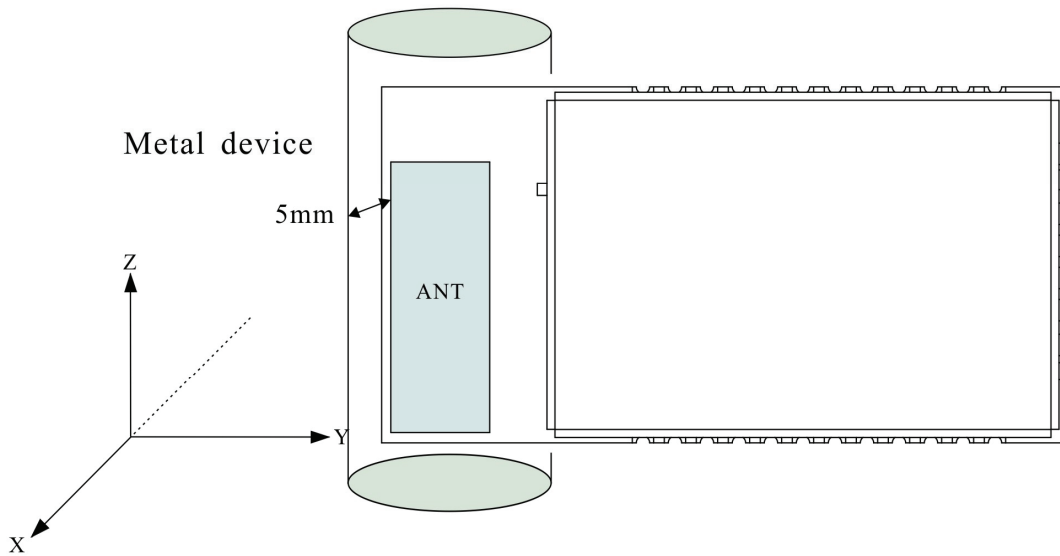


Figure 21: Leave 5mm Clearance Space from the Module Built-in Antenna

9. Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

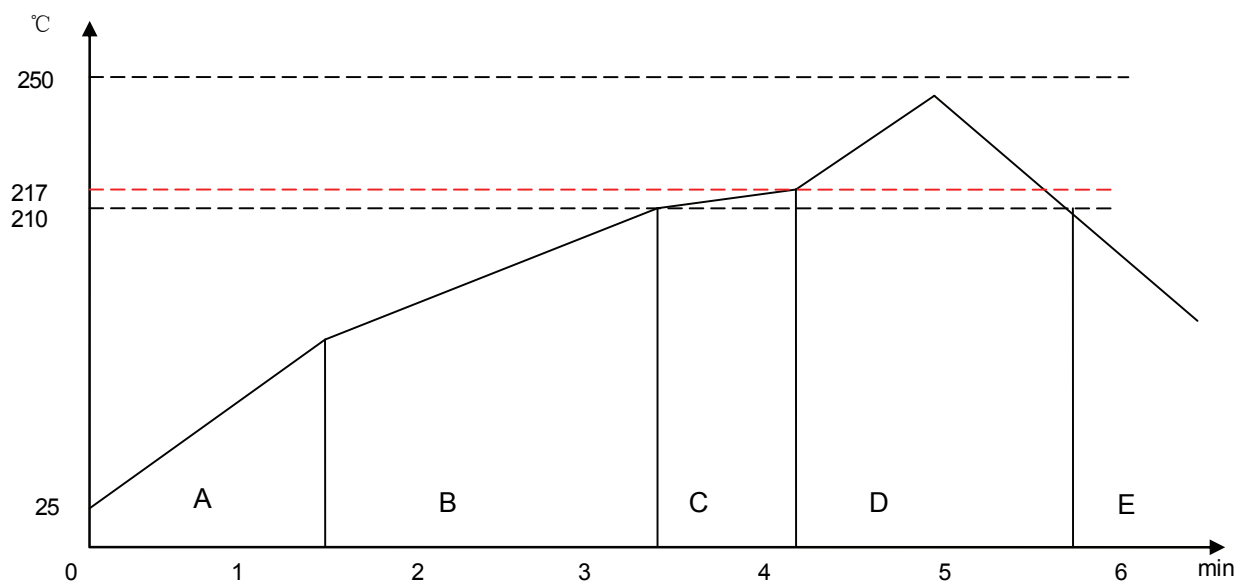


Figure 22: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) — The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint. The recommended peak temperature (Tp) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) — The cooling rate should be fast, to keep the solder grains small which will give a longerlasting joint. **Typical cooling rate should be 4 °C.**

10. Ordering Information

10.1 Product Packaging Information

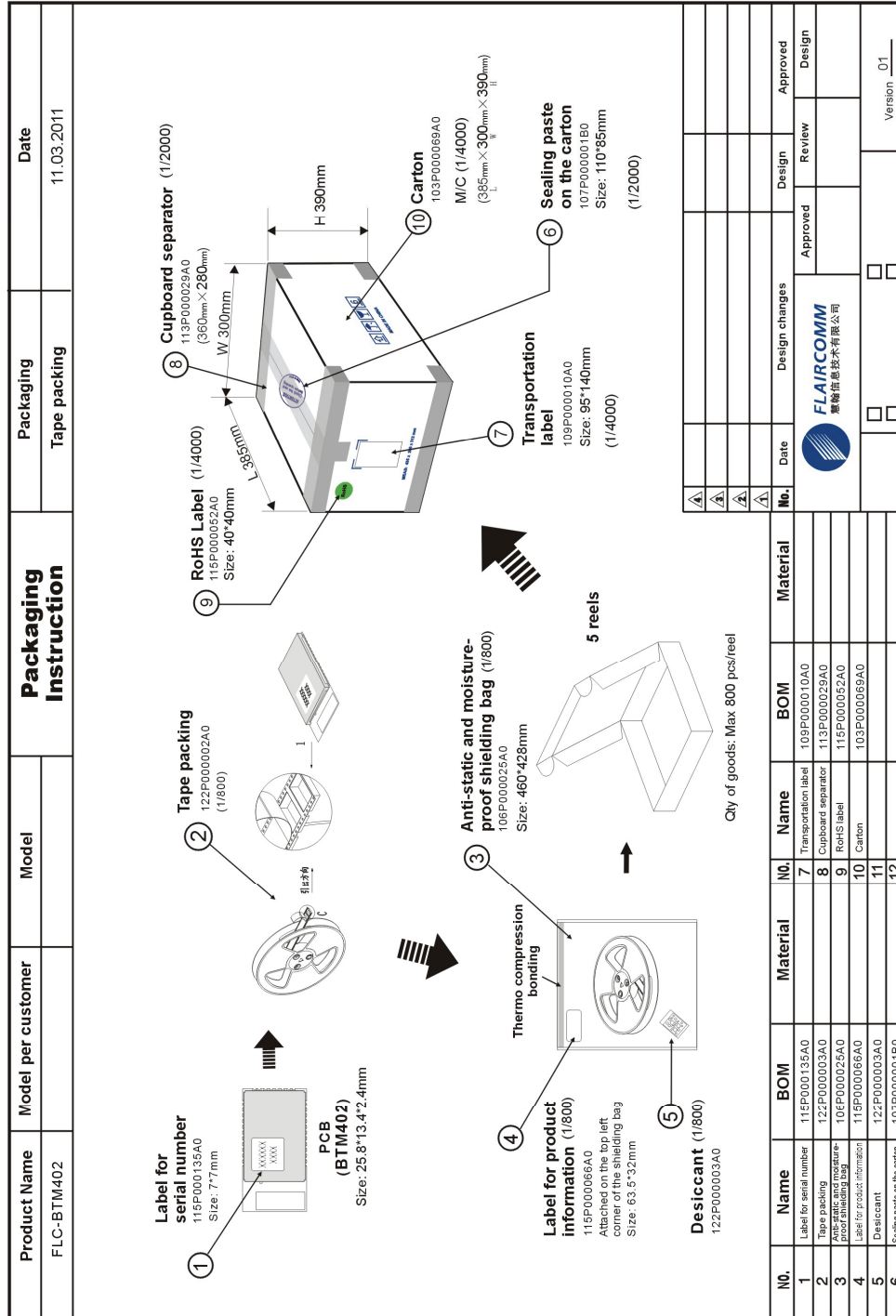


Figure 23: Product Packaging Information

10.2 Ordering Information

FLC-BTM402XYZA



Figure 24: Ordering Information

10.2.1 Product Revision

Product Revision	Description	Availability
A	Release A	Yes

Table 14: Product Revision

10.2.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Form Tray	—	No
1	Plastic Tray	—	No
2	Tape	800x5 = 4000	Yes

Table 15: Shipping Package

10.2.3 Product Package

Product Package	Description	Availability
Q	QFN	Yes
L	LGA	No
B	BGA	No
C	Connector	No

Table 16: Product Package

10.2.4 Product Grade

Product Grade	Description	Availability
C	Consumer	Yes
I	Industrial	Yes
V	Automobile After-Market	Yes
A	Automobile Before-Market	No

Table 17: Product Grade